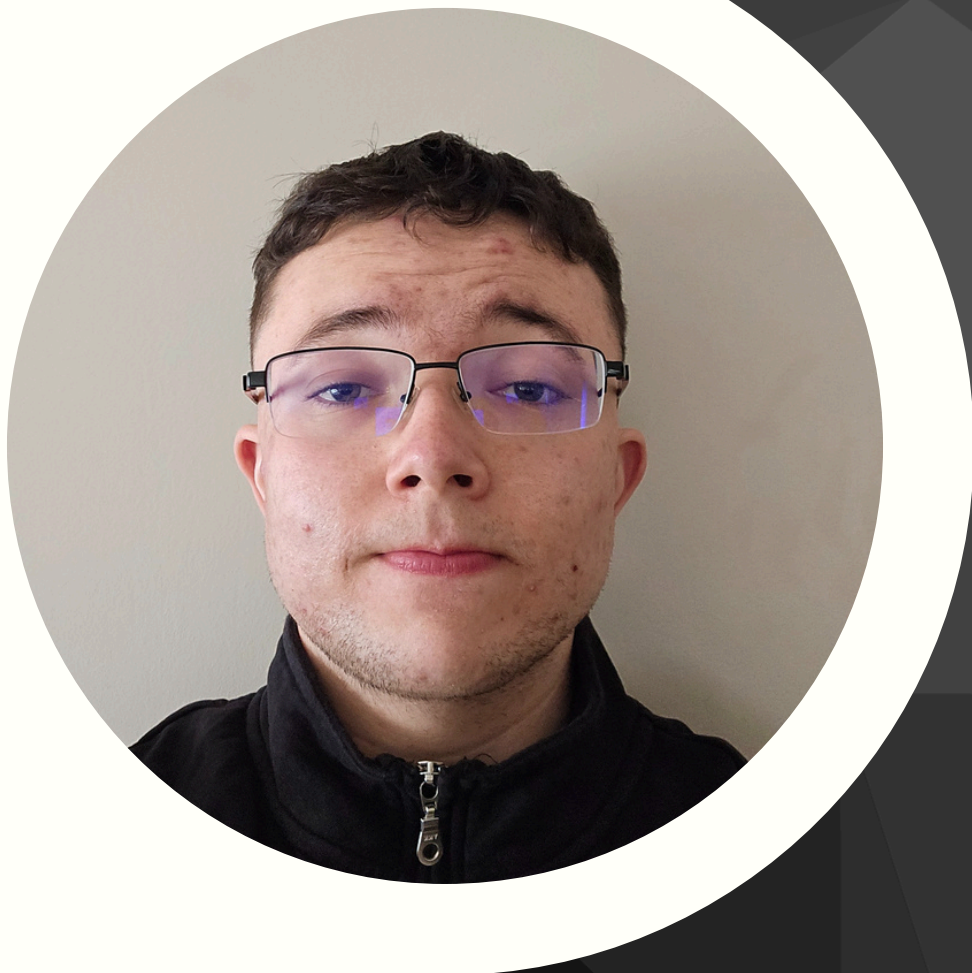


# PORT FOLIO

By Nick Rathfelder

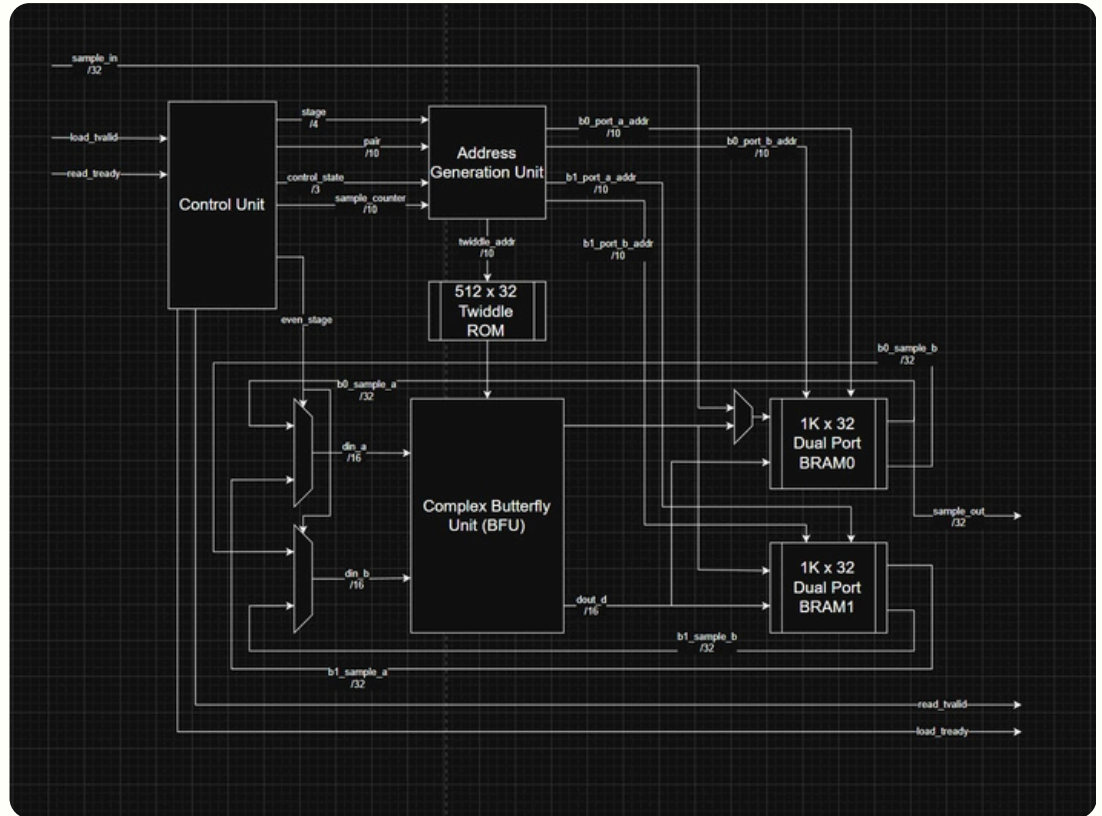


Electrical Engineering  
2022 - 2027

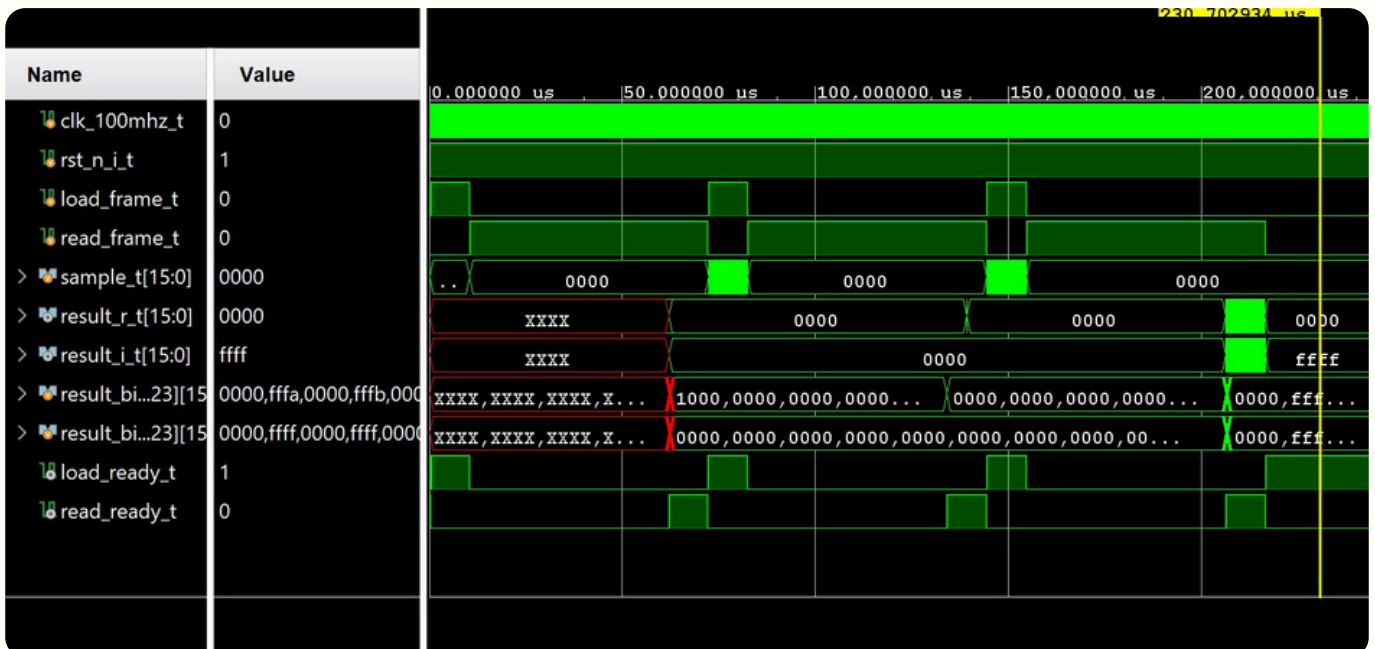
# **MAIN PROJECTS**

# FFT CORE

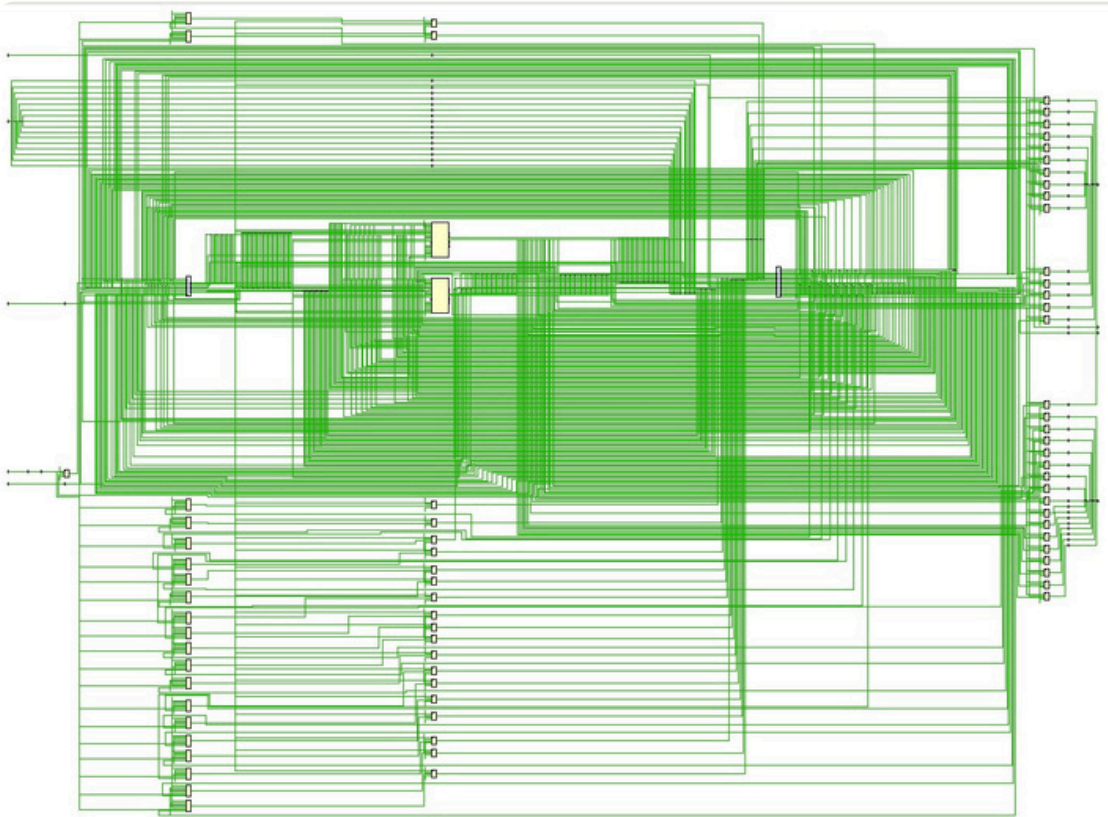
Top Level Block Diagram



Simulation Waveform

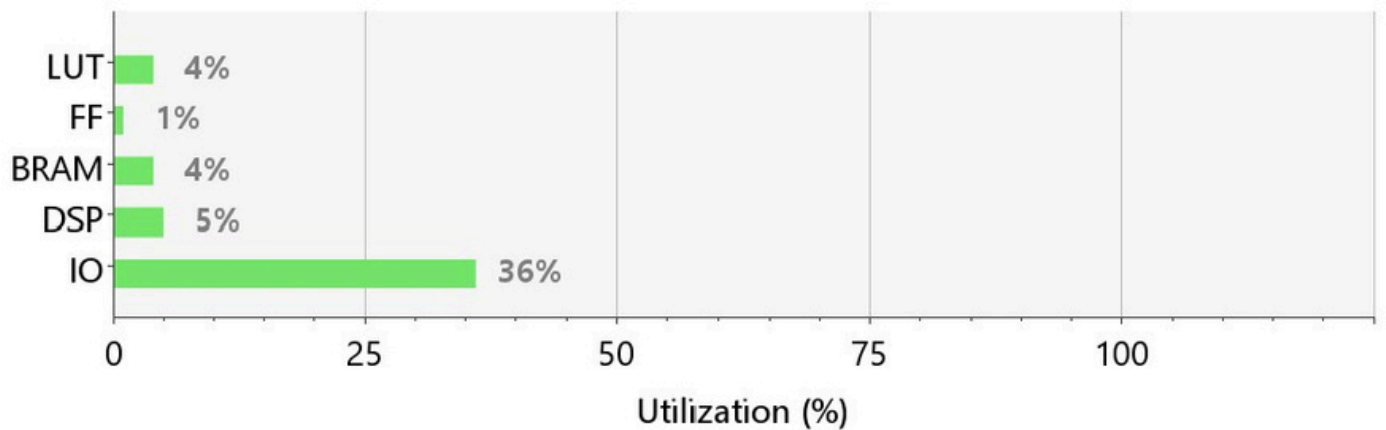


# SYNTHESIS

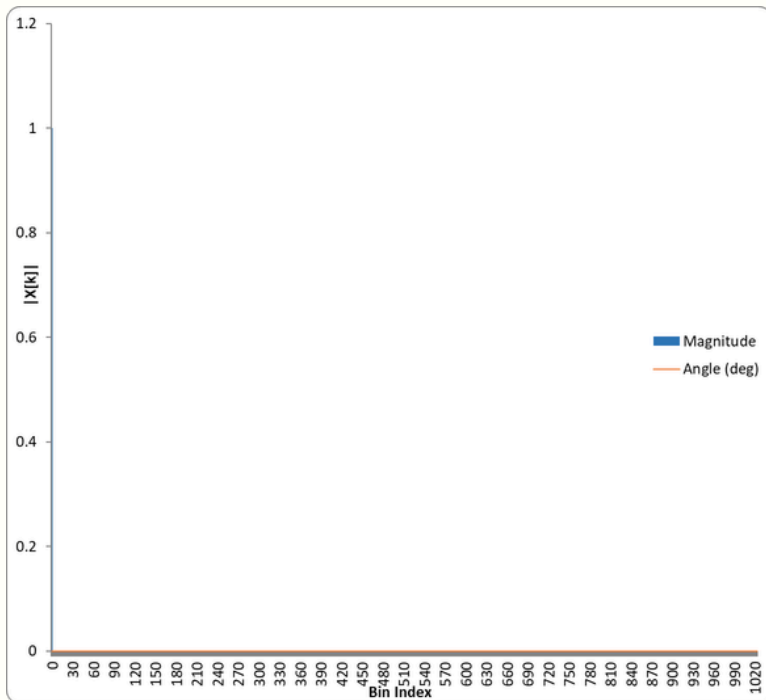


Synthesized  
Design

## Resource Utilization

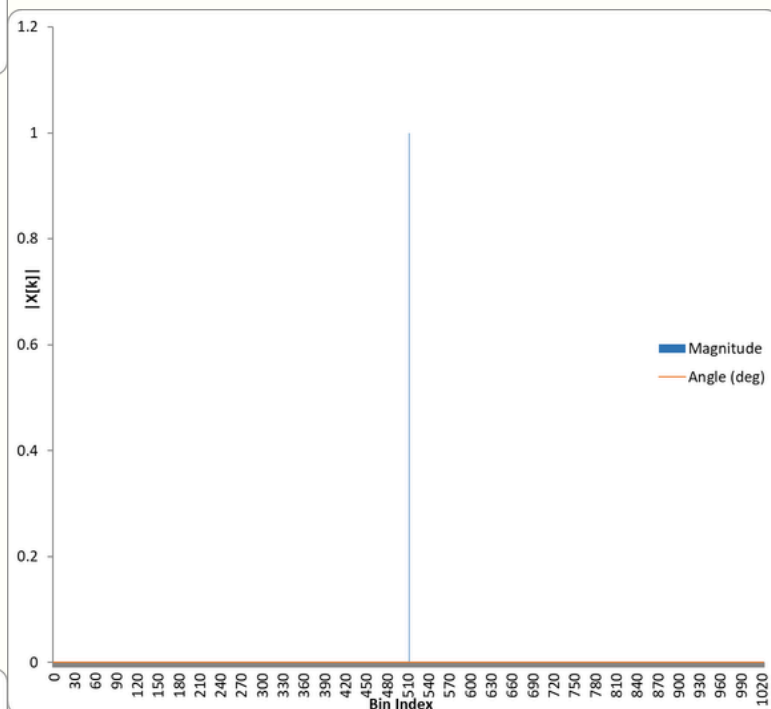


# SIMULATION

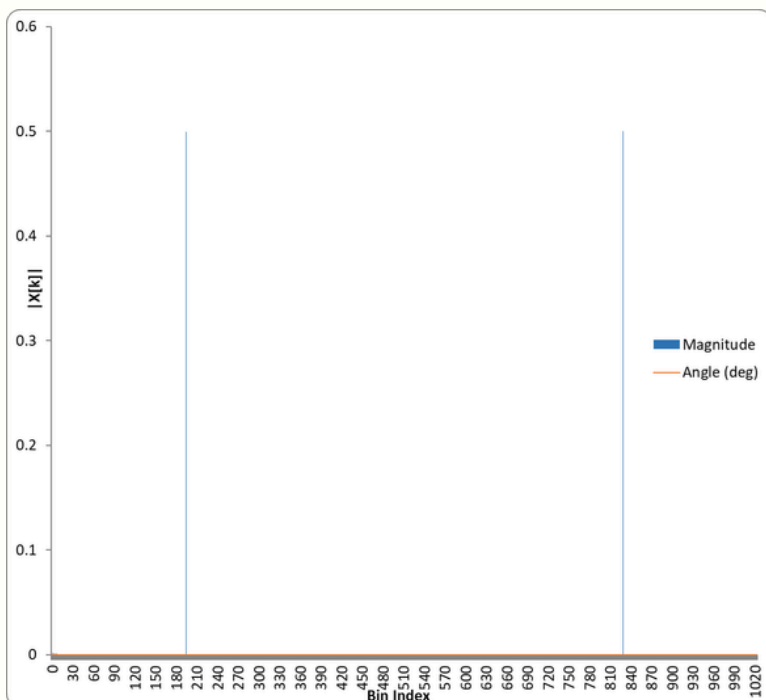


Constant DC

Nyquist  
Sinusoid

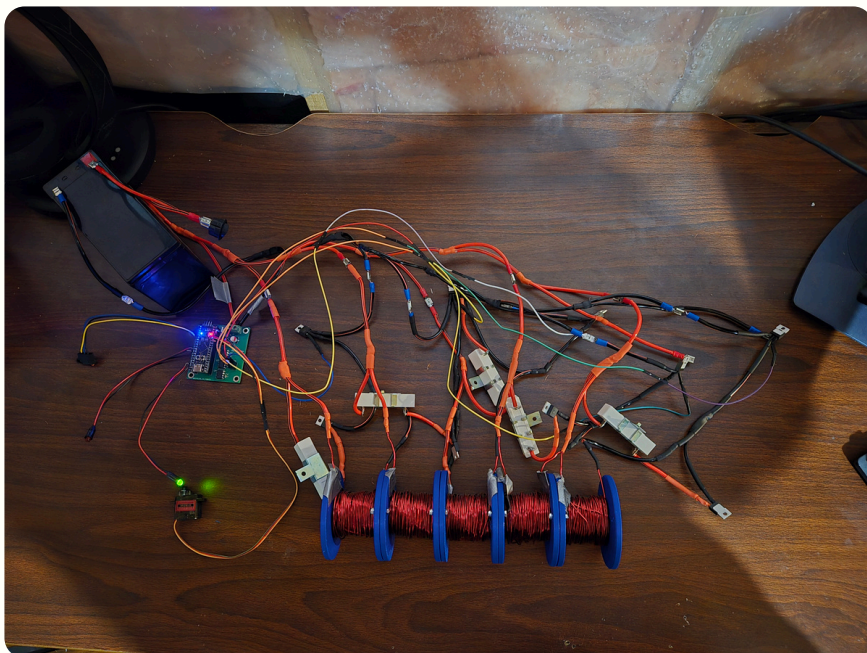
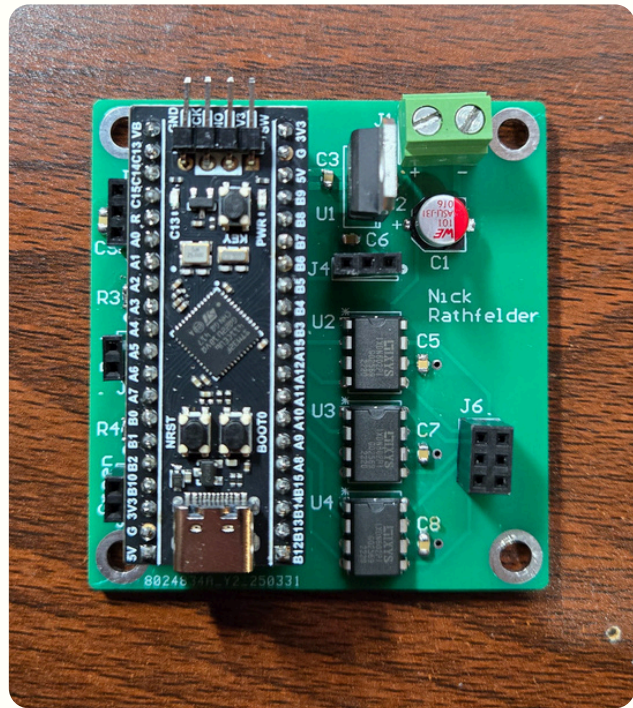


Custom  
Sinusoid  
(Bin 195)



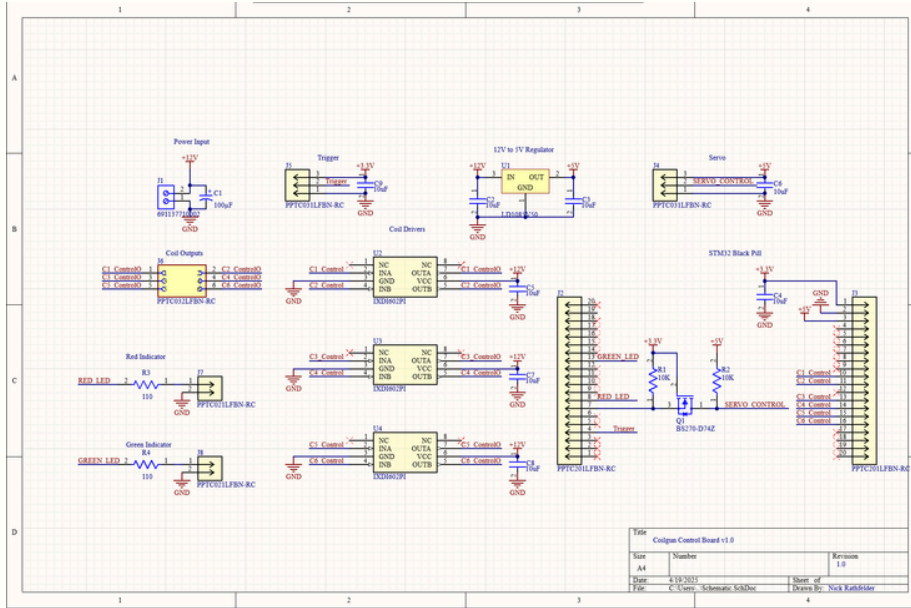
# ELECTROMAGNETIC LAUNCHER

STM32  
Interface PCB



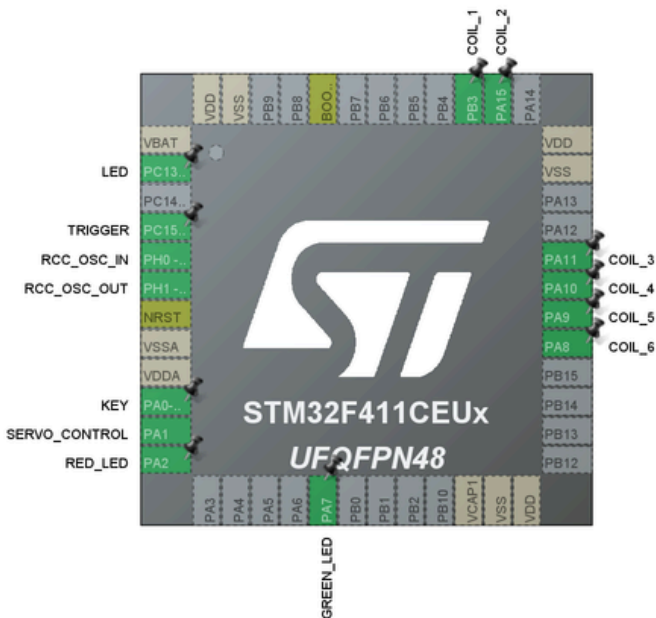
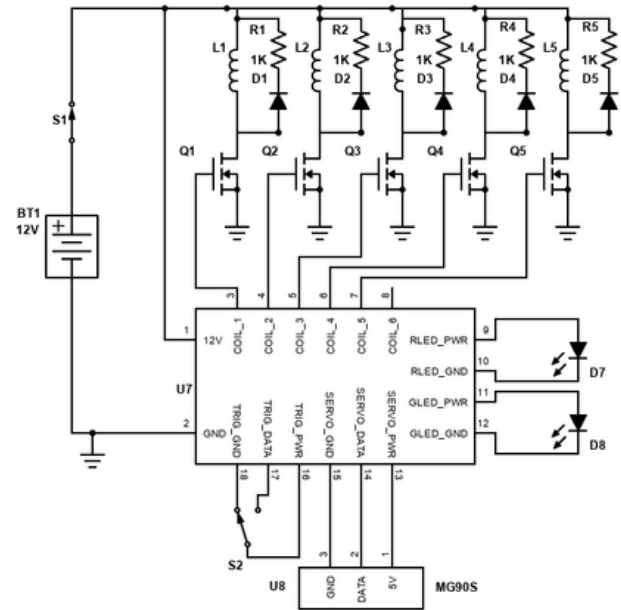
Final Prototype

# DESIGN



## Interface PCB Schematic

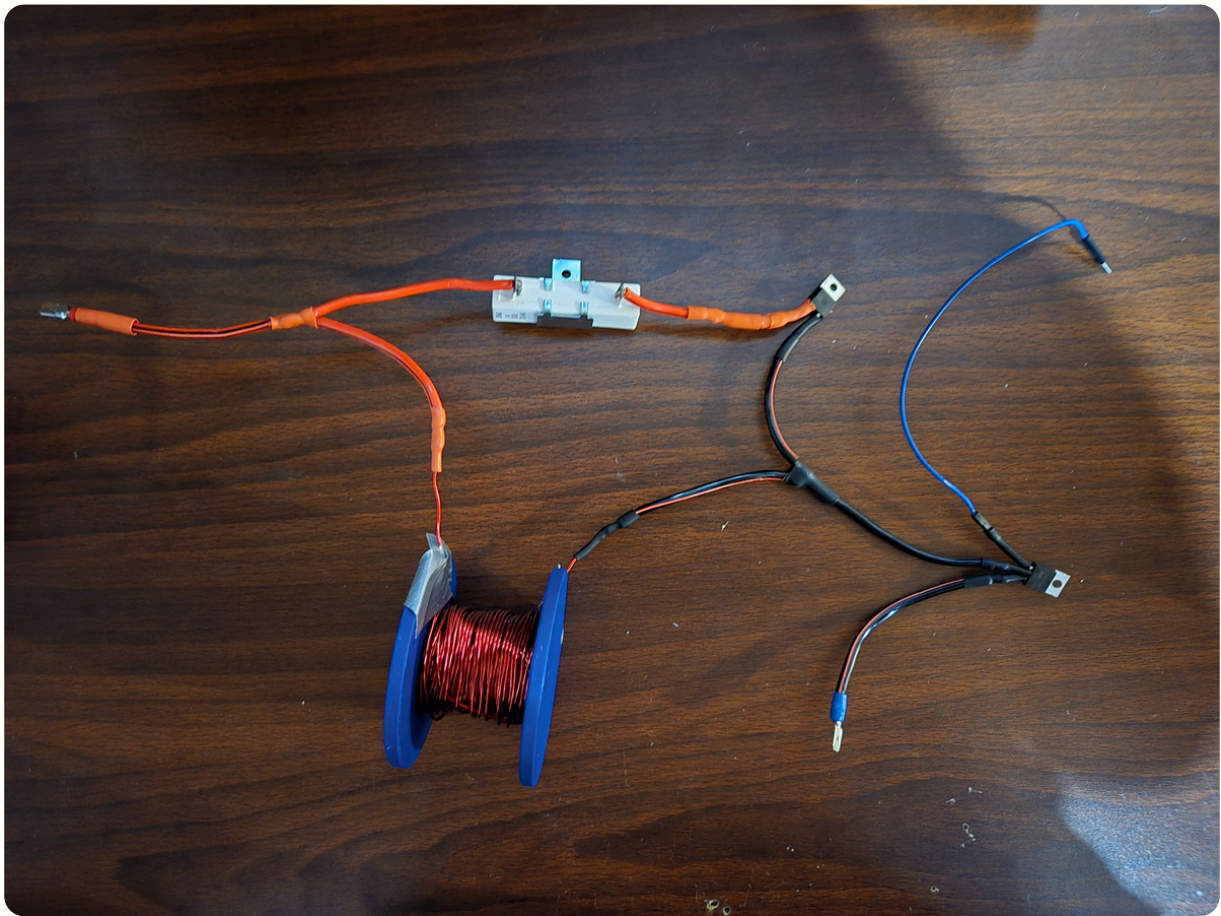
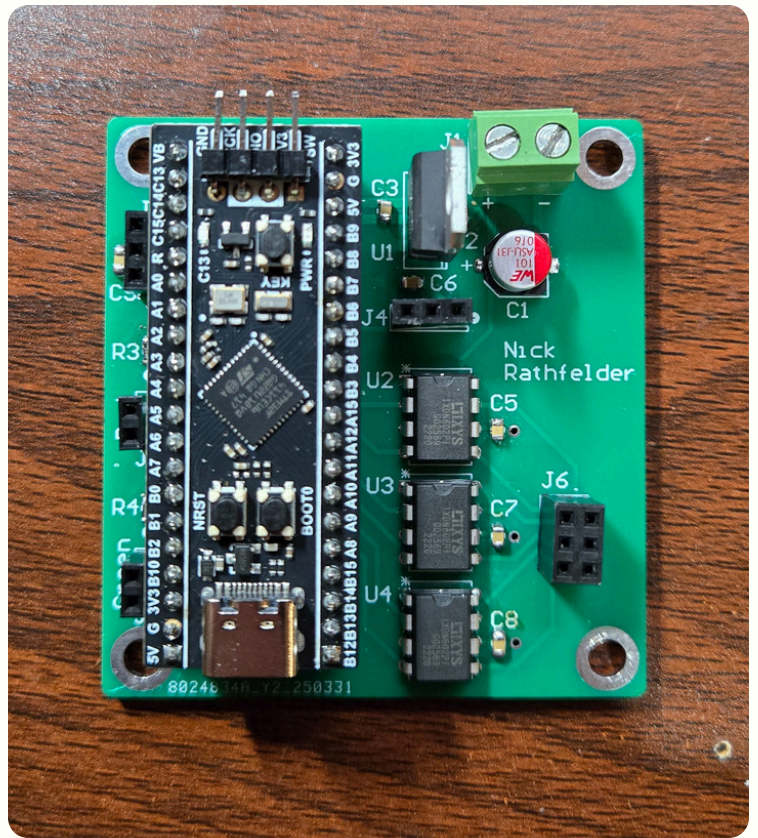
## Wire Harness Schematic



## MCU Pin Configuration

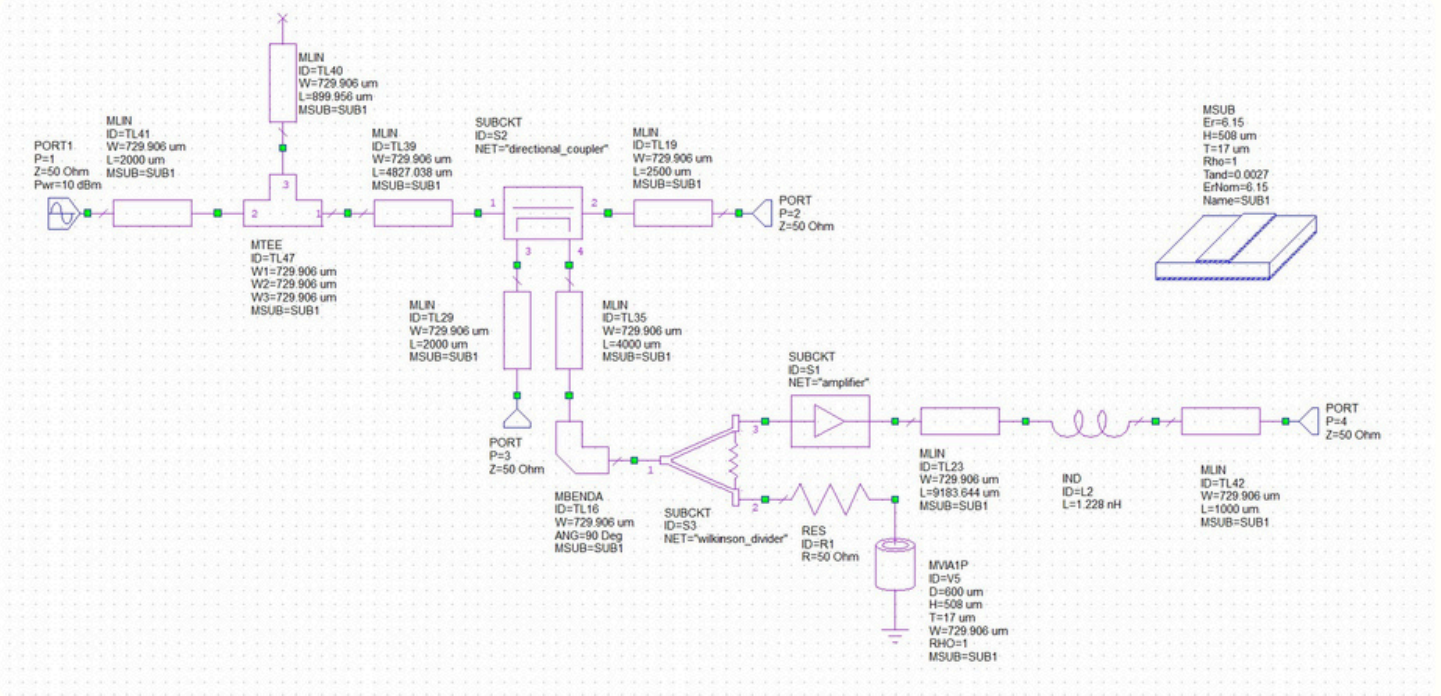
# PROTOTYPE

Assembled  
Control PCB



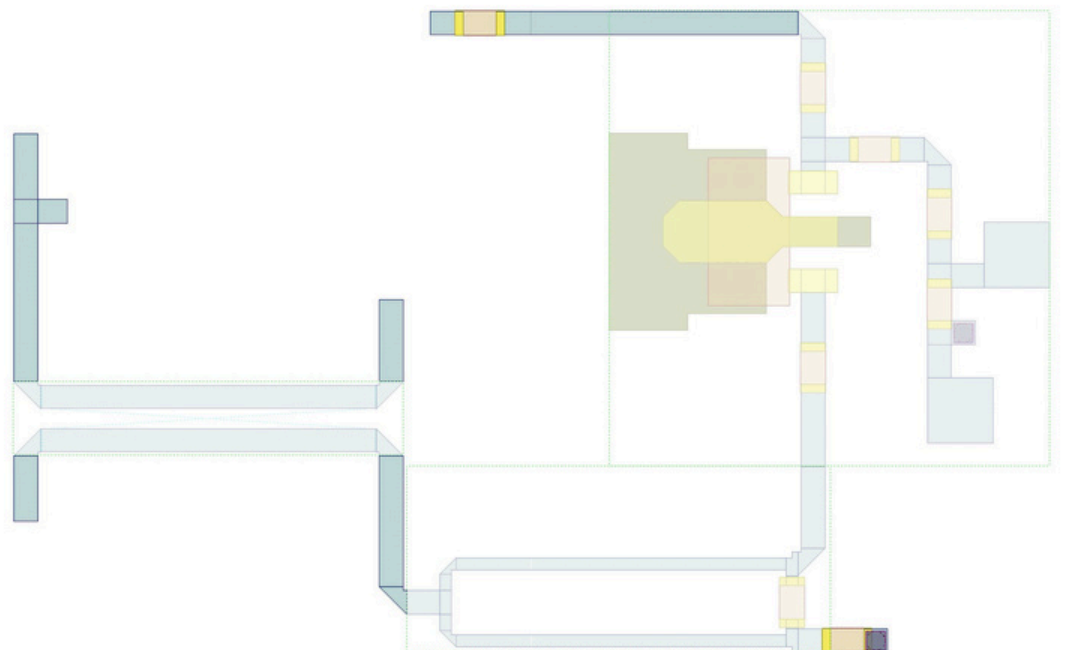
Single Coil Stage

# RF REFLECTOMETER

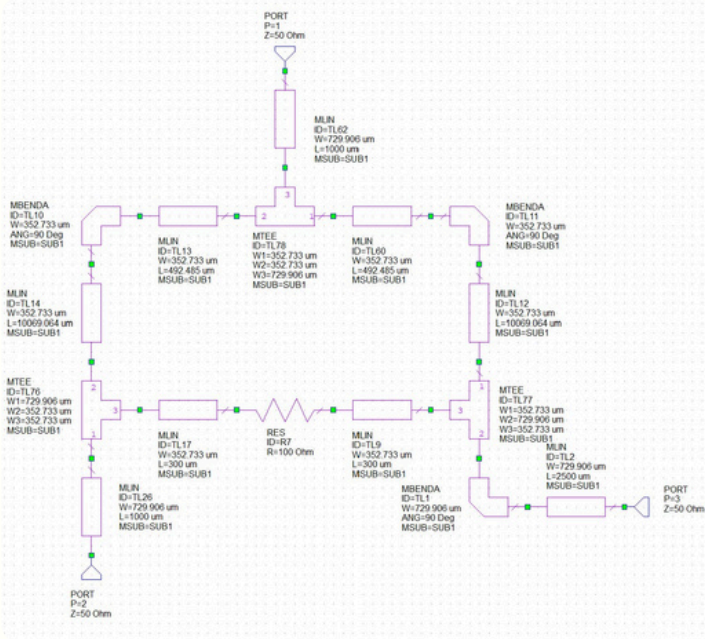


Top Level Schematic

Layout

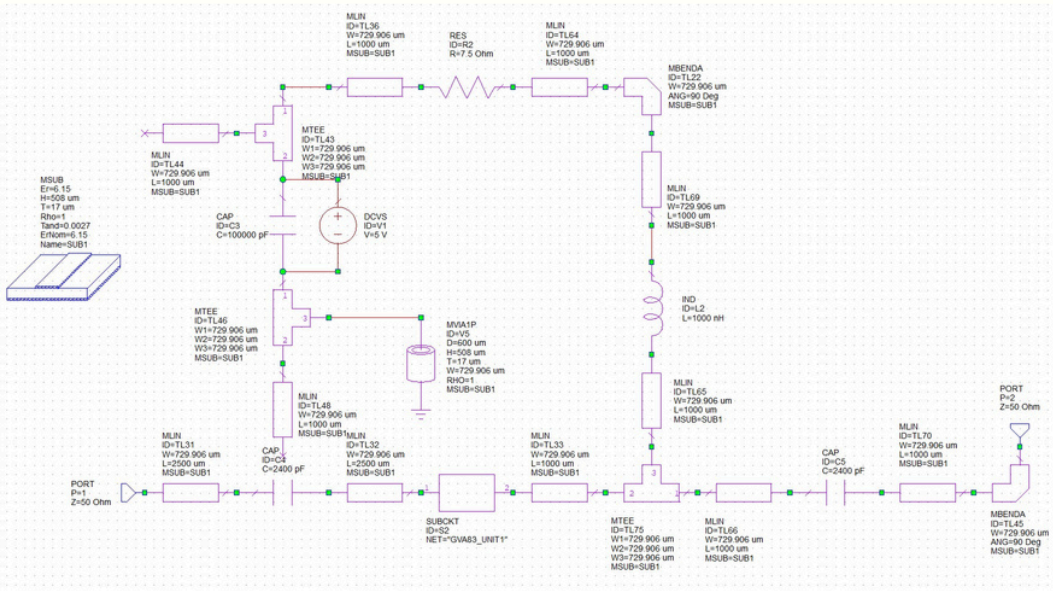
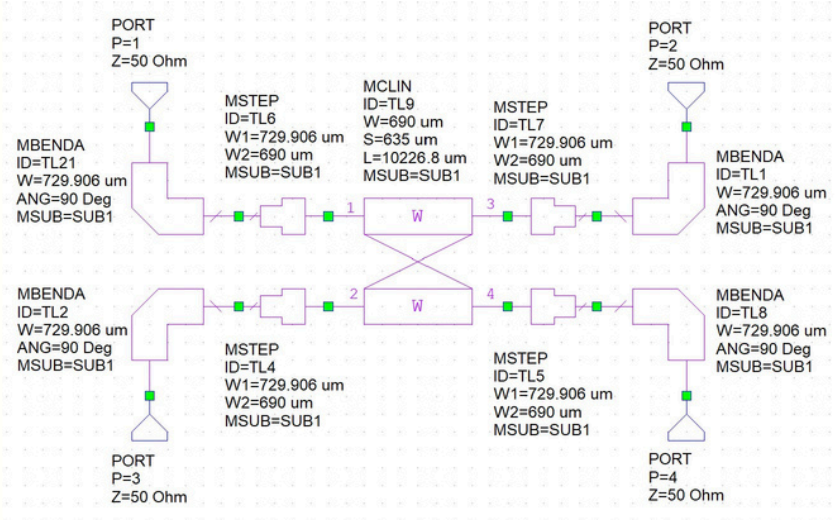


# SCHEMATICS



Wilkinson  
Divider

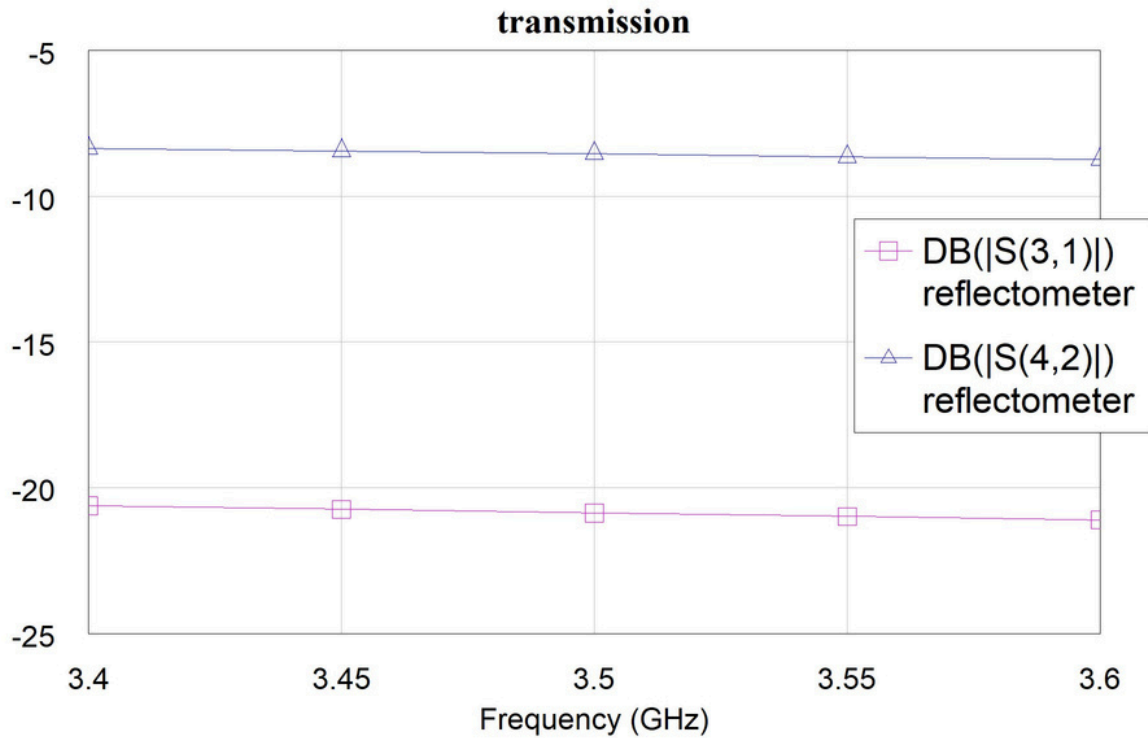
Directional  
Coupler



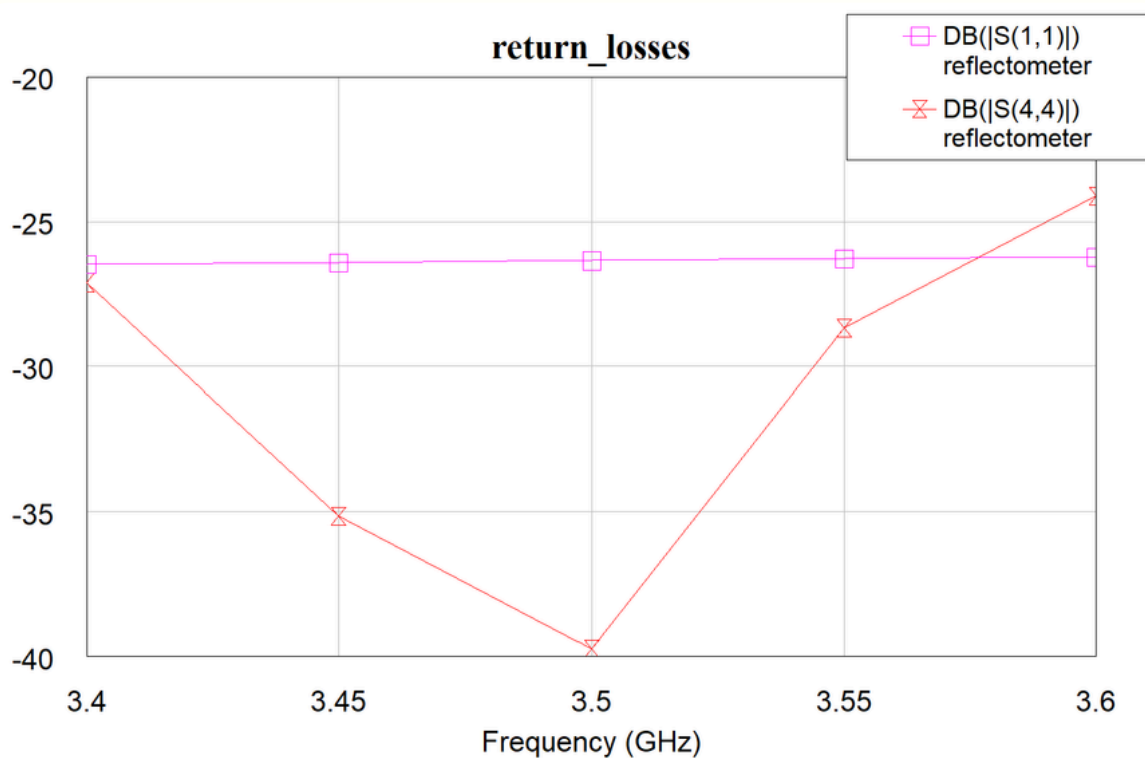
Amplifier

# SIMULATION

## Forward/Reflected Output Gain

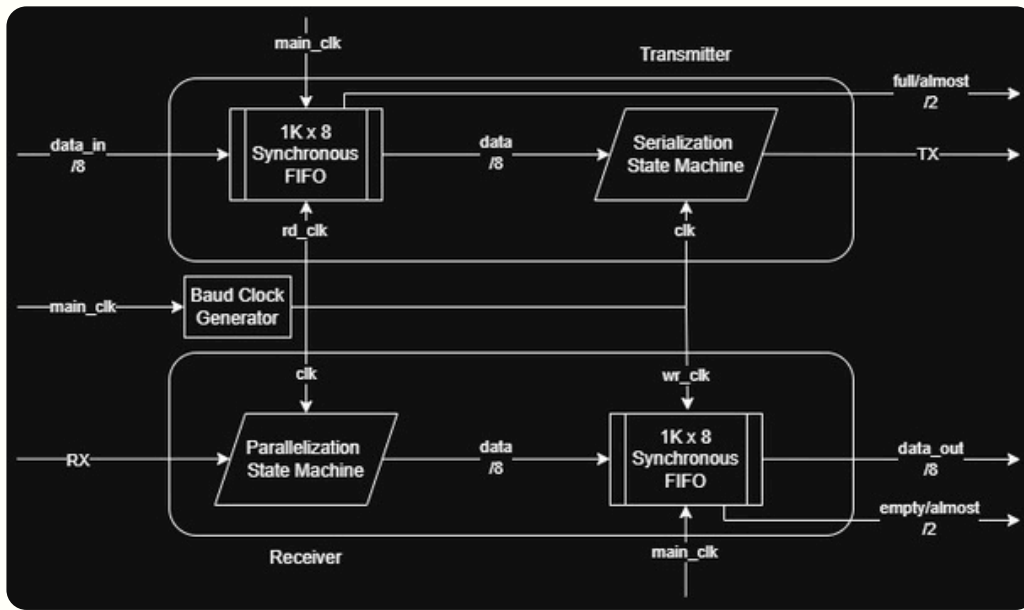


## Input/Output Return Losses



# **SIDE PROJECTS**

# UART CORE + DEBUG PORT



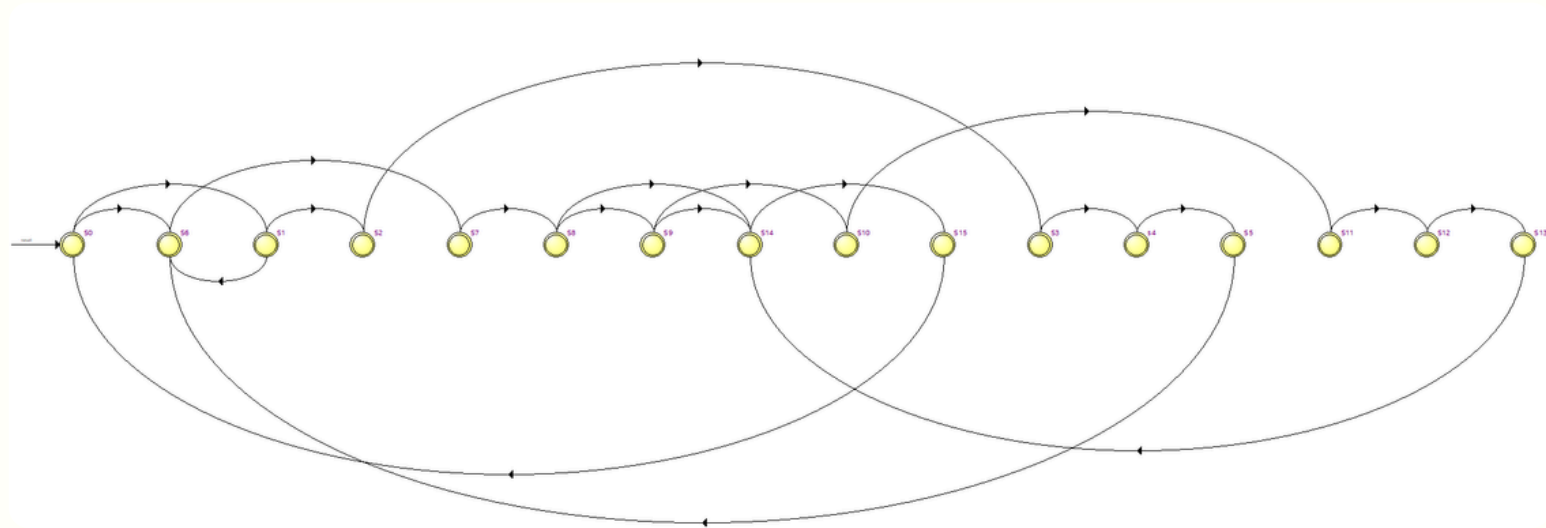
Block Diagram  
(Core only)

Terminal  
Output

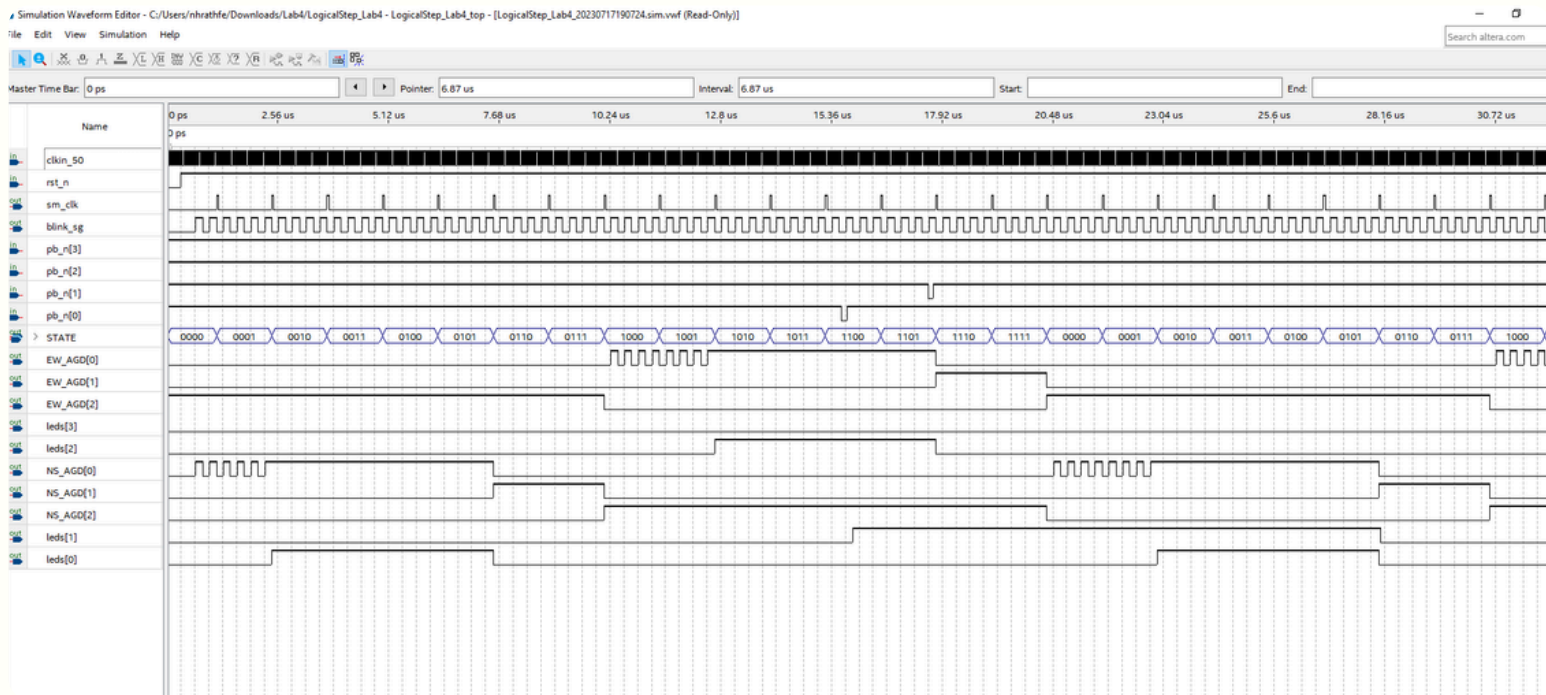
```
COM5 - Tera Term VT
File Edit Setup Control Window Help
MESSAGE_0_SENT
MESSAGE_1_SENT
MESSAGE_2_SENT
MESSAGE_3_SENT
MESSAGE_4_SENT
MESSAGE_5_SENT
MESSAGE_6_SENT
MESSAGE_7_SENT
MESSAGE_8_SENT
MESSAGE_9_SENT
MESSAGE_10_SENT
MESSAGE_11_SENT
MESSAGE_12_SENT
MESSAGE_13_SENT
MESSAGE_14_SENT
MESSAGE_15_SENT
```

# FPGA TRAFFIC LIGHT CONTROLLER

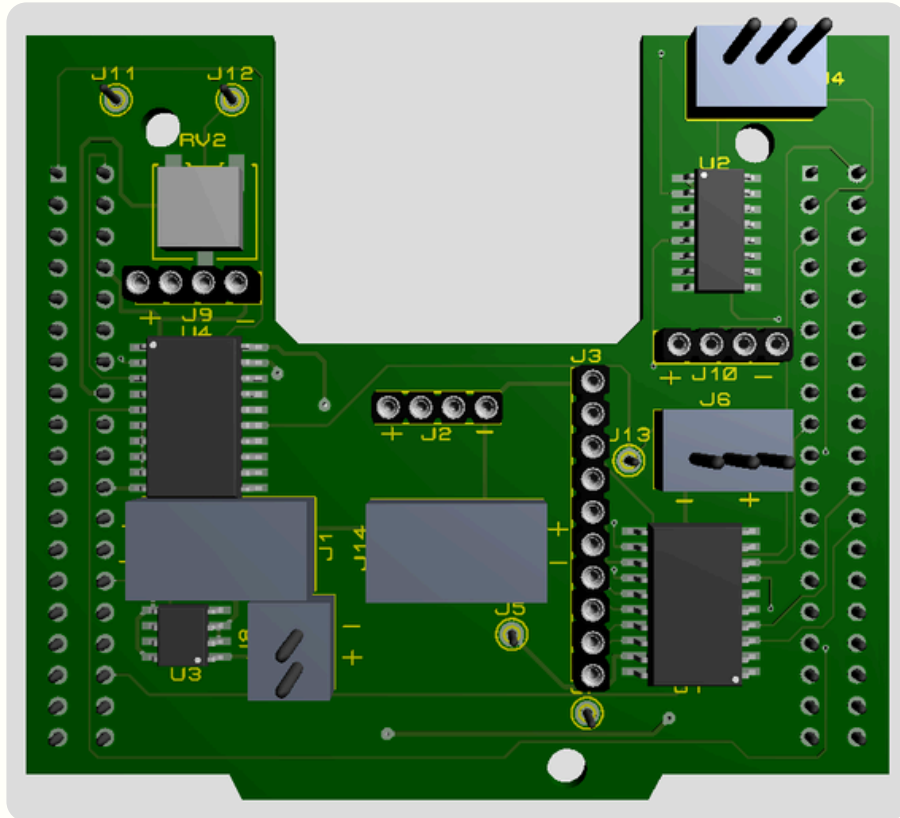
## Controller State Machine



## Testbench Waveform

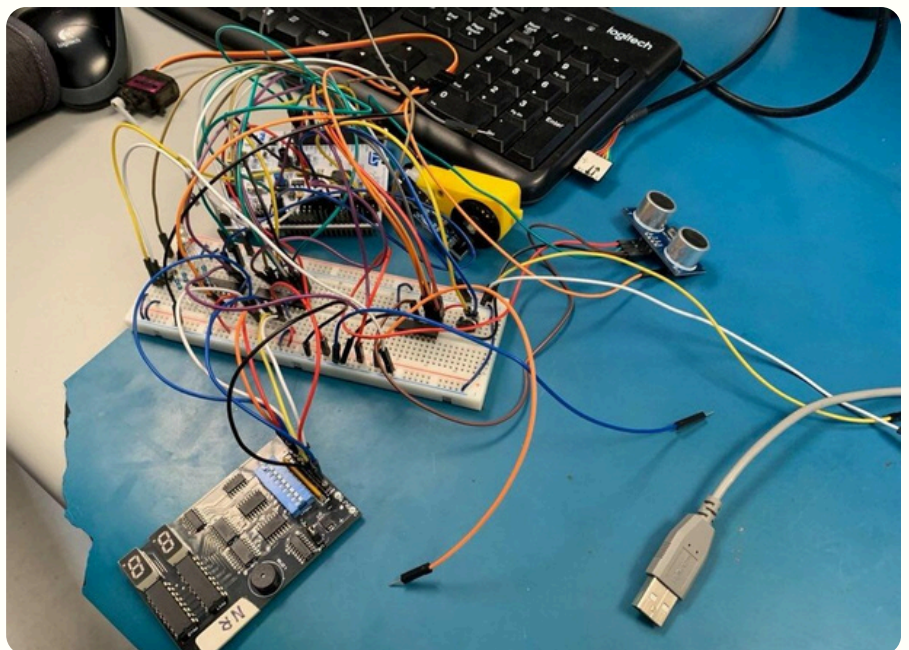


# WATER RESERVOIR CONTROL SYSTEM



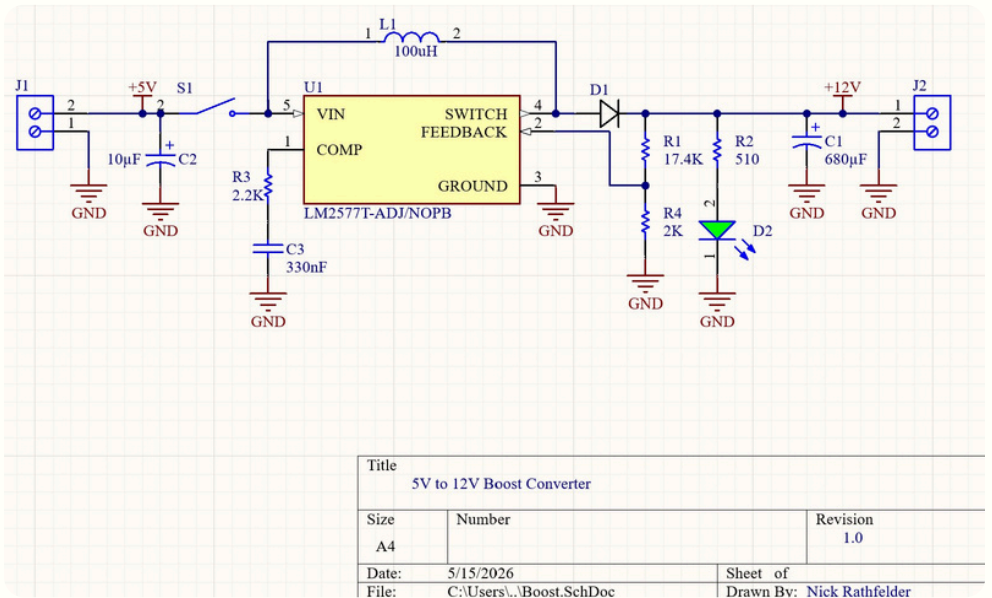
Interface PCB

Functional Prototype

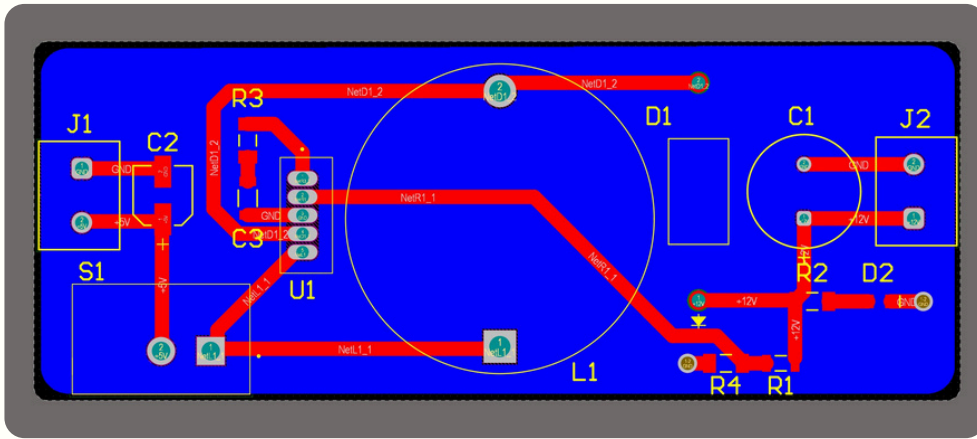


# 5V-12V BOOST CONVERTER PCB

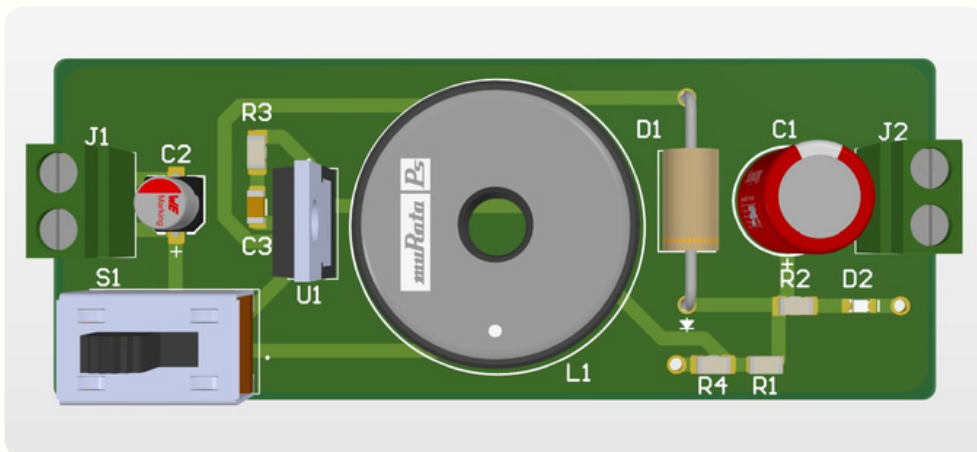
Schematic



Layout

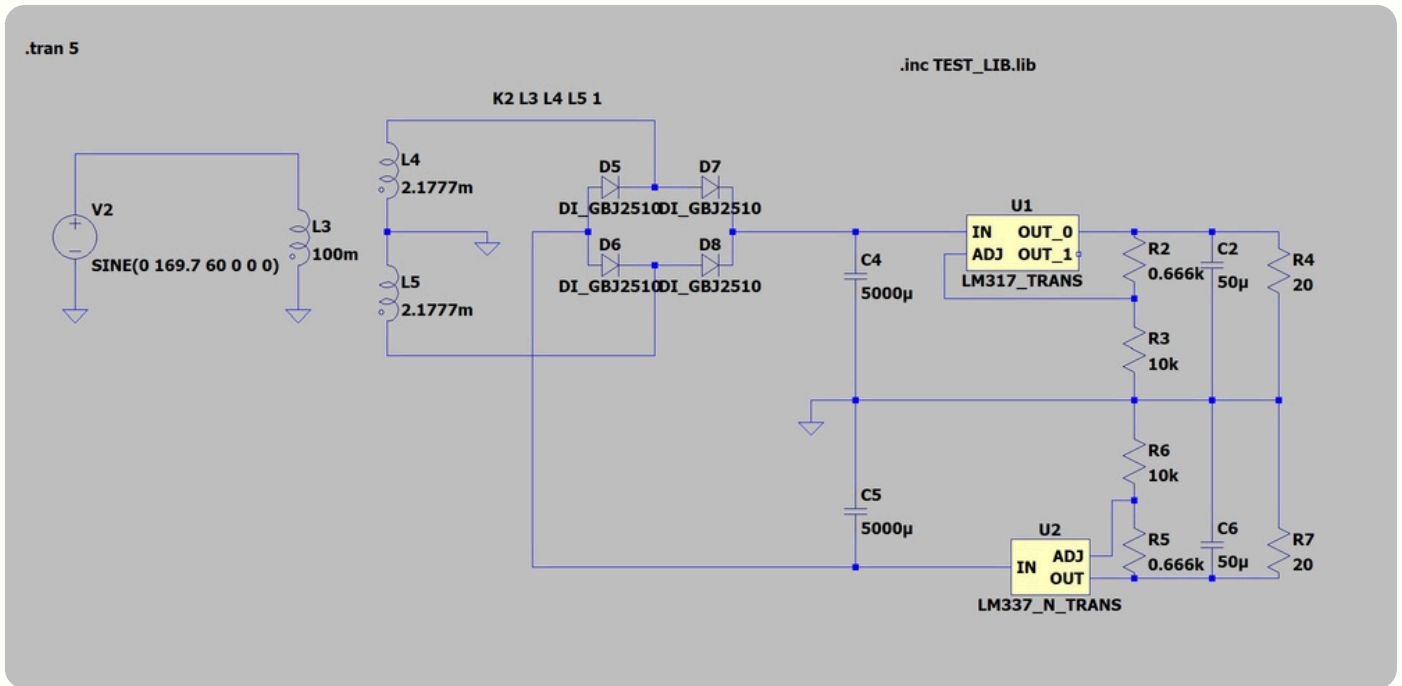


Model



# SIMULATED DUAL OUTPUT AC-DC PSU

## Schematic



## Simulation

