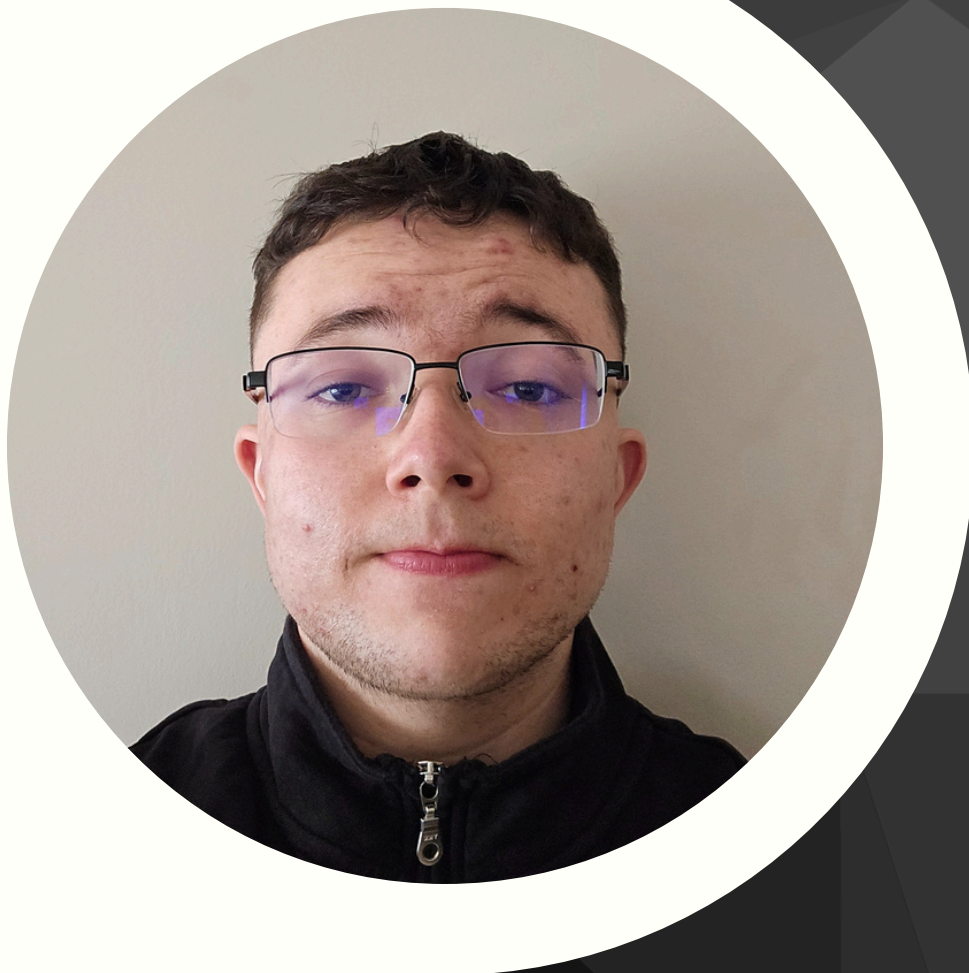


PORT FOLIO

By Nick Rathfelder

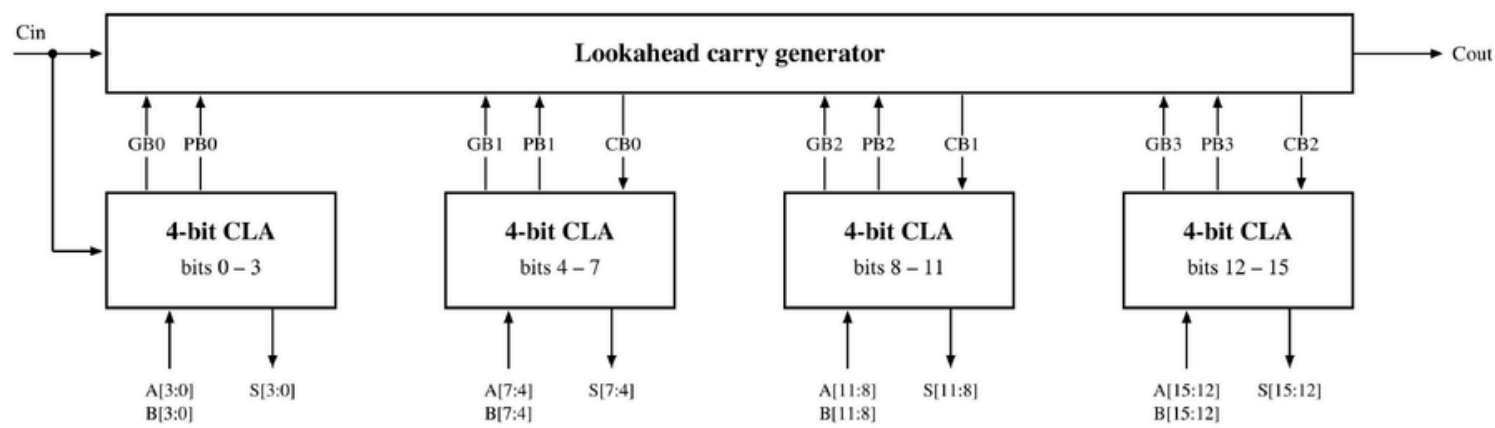


Electrical Engineering
2022 - 2027

MAIN PROJECTS

16-BIT CMOS CARRY-LOOKAHEAD ADDER

Top Level Block Diagram



Final Comparison Results

16-bit CLA Adder: Results

Static CMOS, 45 nm (GPDK045), nominal VDD = 1.1 V, 1 ns addition-time spec

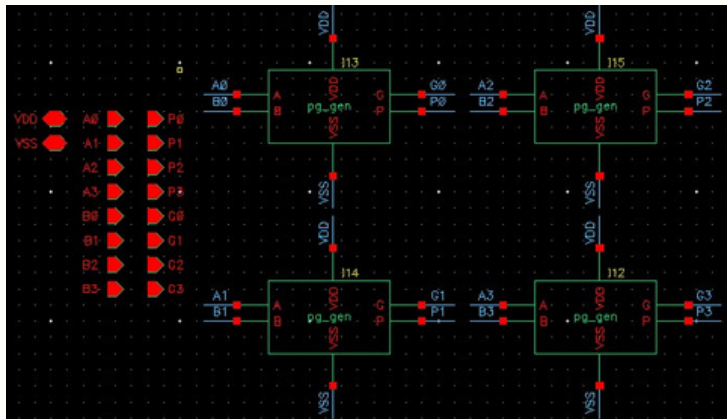
CLA vs. ripple-carry (RCA)				
worst-case vector A, TT, 27 °C				
	Transistors	Delay (ps)	Power (µW)	PDP (fj)
RCA	448	1008	123.1	124.1
CLA	988	456	300.1	136.9
CLA vs. RCA	2.2x	-55%	2.4x	+10%

CLA delay across corners (ps)			
all three test vectors			
	FF -25 °C	TT 27 °C	SS 85 °C
Vector A FFFF + 0001	312.7	456.0	676.5
Vector B FFFF + FFFF	216.9	312.0	459.2
Vector C AAAA + AAAA	214.4	308.0	453.3
All cases meet the 1 ns spec (worst case 676.5 ps, outlined)			

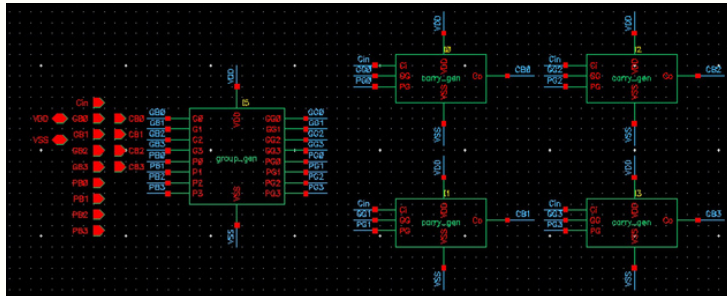
Process Technology - 45nm (GPDK045)

SCHEMATICS

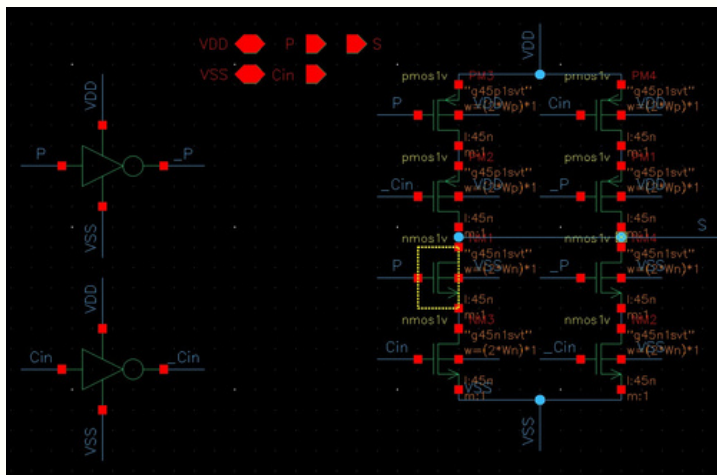
Setup



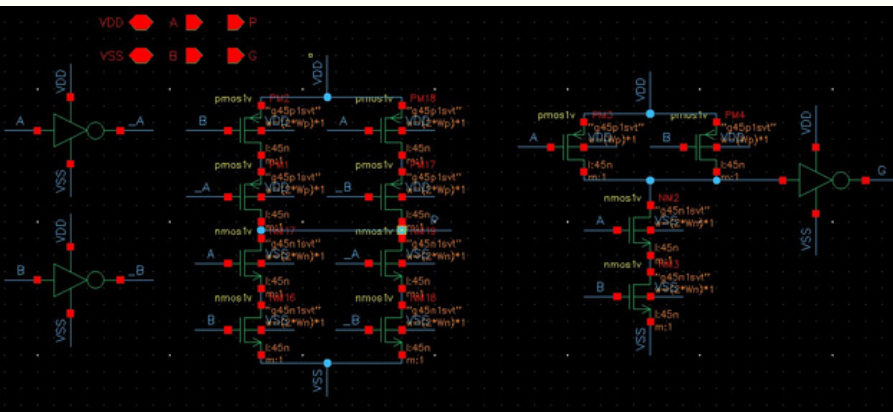
Intermediate Carry Generation



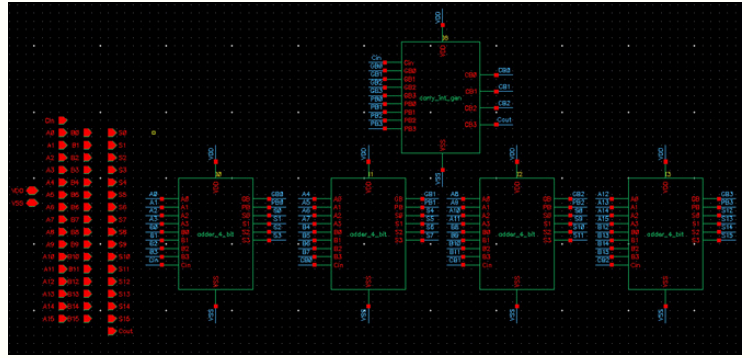
Sum Generation



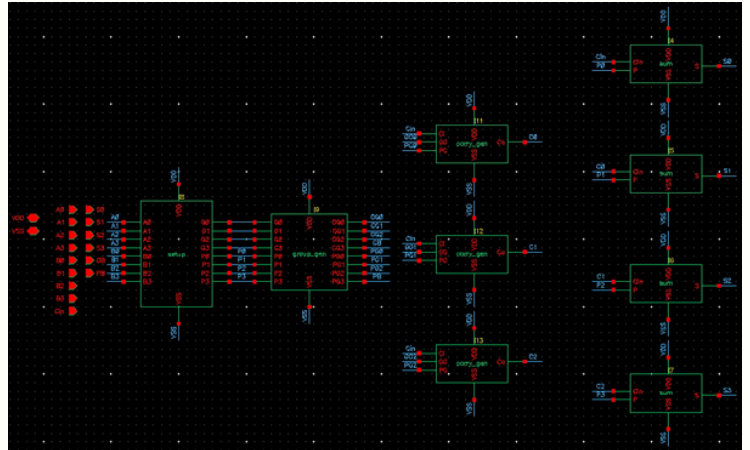
Propagate/Generate Synthesis



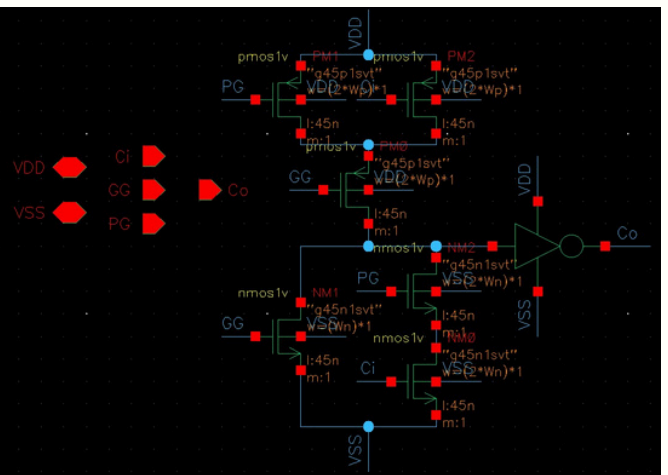
16-Bit Adder Schematic



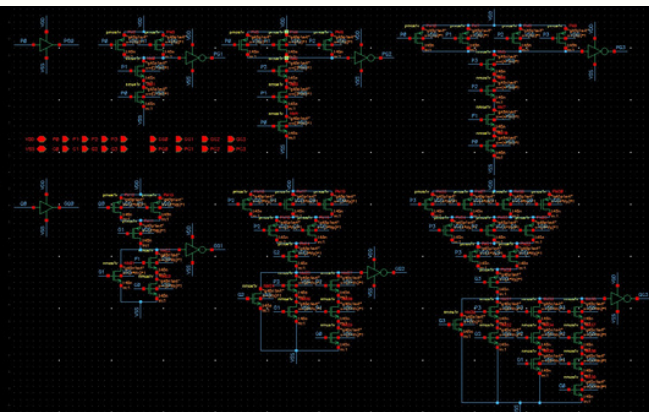
4-Bit Adder Schematic



Carry Out Generation



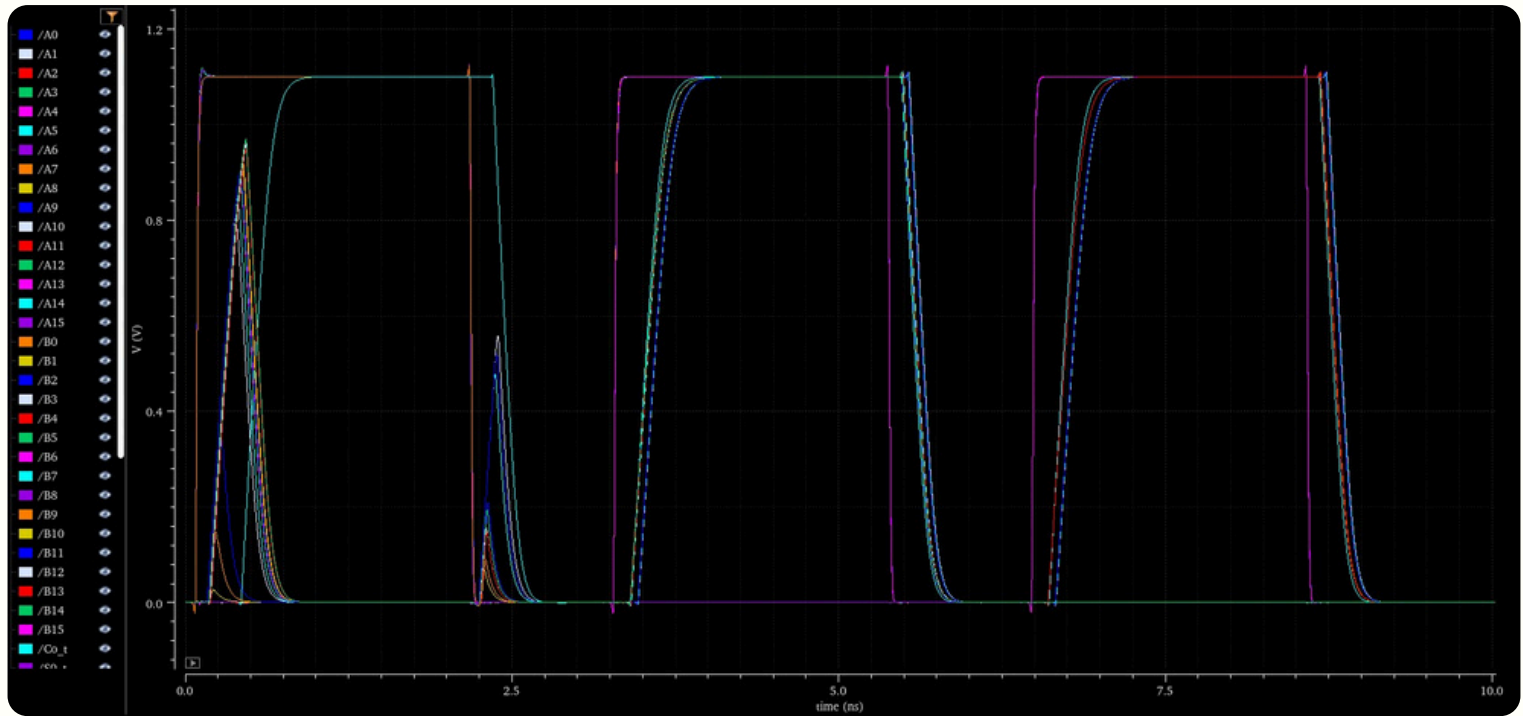
Group P/G Generation



Sizing: $W_n = 120 \text{ nm}$ and $W_p = 140 \text{ nm}$, tuned empirically to equalize rise/fall times. Series stacks are scaled by depth (2x, 3x, 4x)

SIMULATION

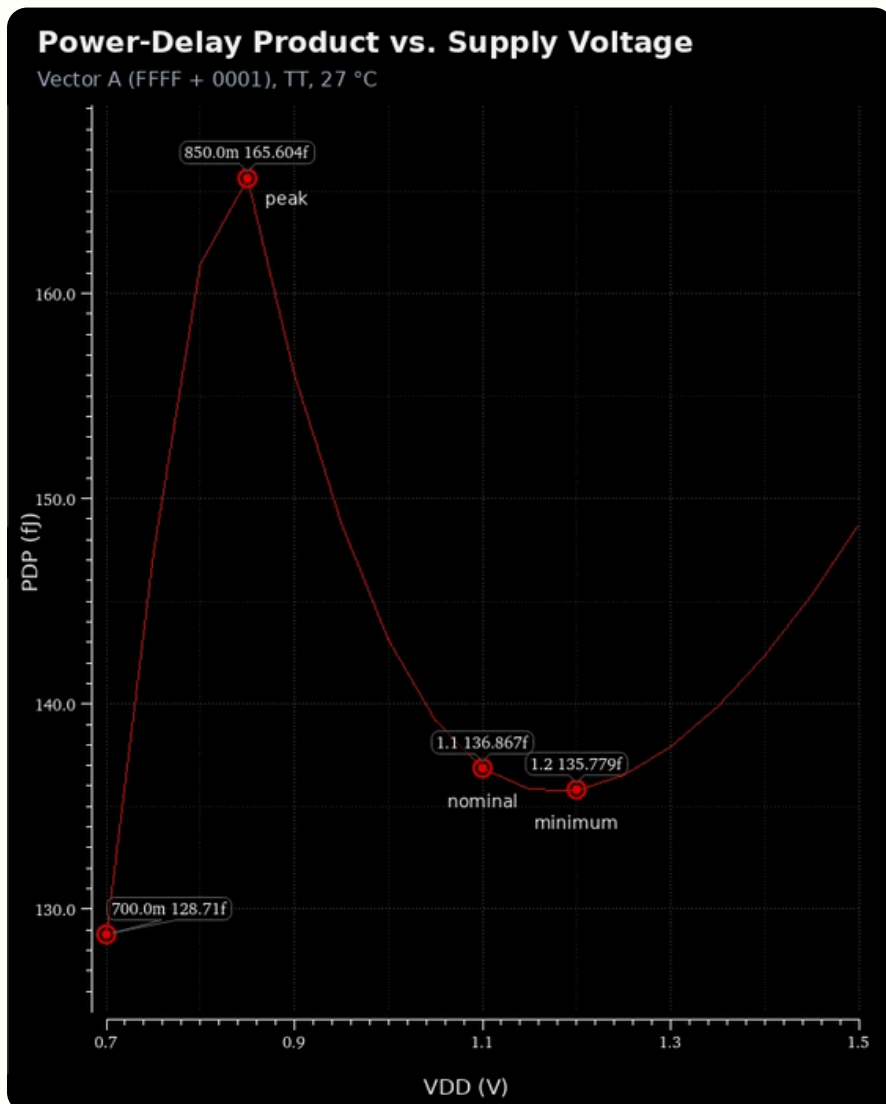
Functional Simulation



Vector A (FFFF + 0001)

Vector B (FFFF + FFFF)

Vector C (AAAA + AAAA)

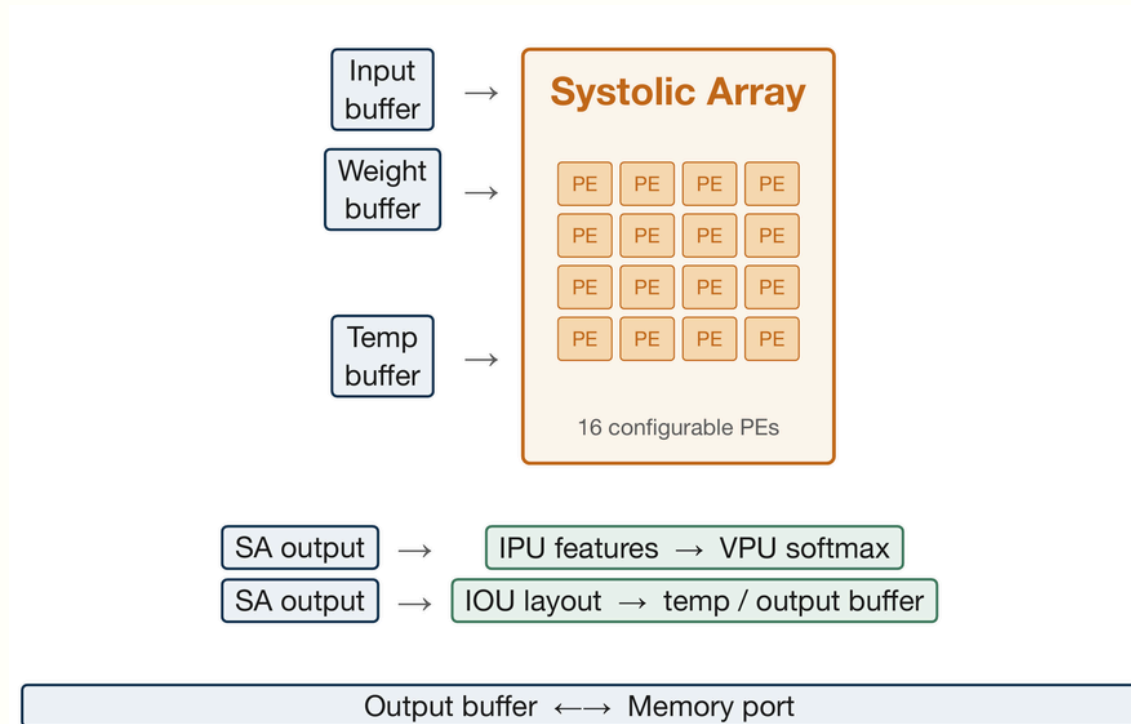


Power-Delay-Product
(PDP) vs VDD

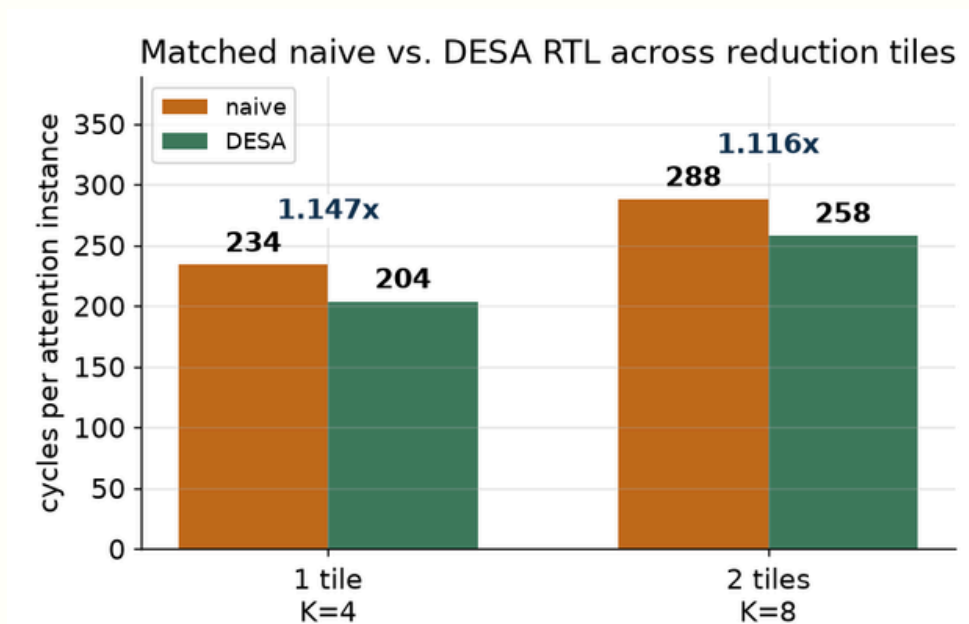
DESA-BASED RUNTIME CONFIGURABLE SYSTOLIC ARRAY

Reduced-scale RTL reproduction of DESA (Wang et al., IEEE Trans. Computers, 2025). Team project of five; I designed the systolic array and mode-wave RTL.

System Architecture



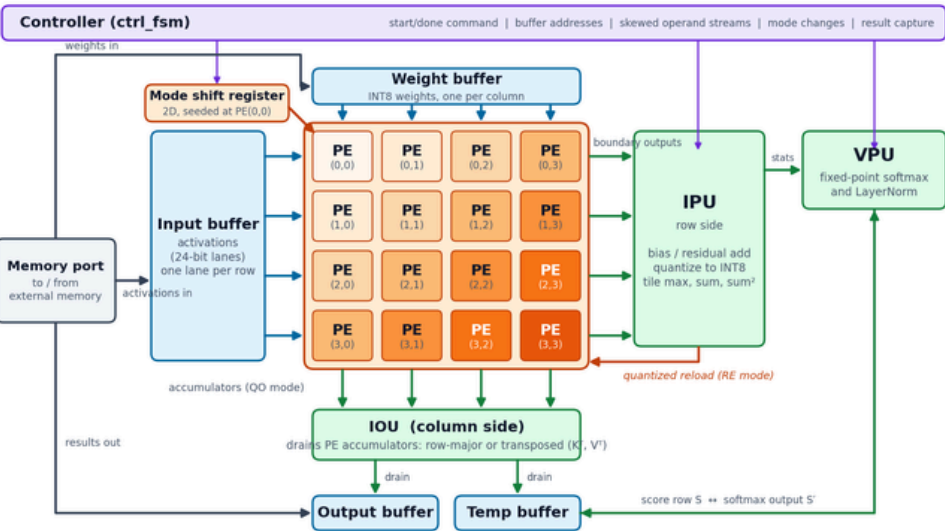
Measured Cycle Reduction



ARCHITECTURE

Reduced-Scale Runtime-Configurable Systolic Array: Block Diagram

4 × 4 grid of configurable PEs with the mode wave, buffers, and side units (IPU, IOU, VPU) wired around it

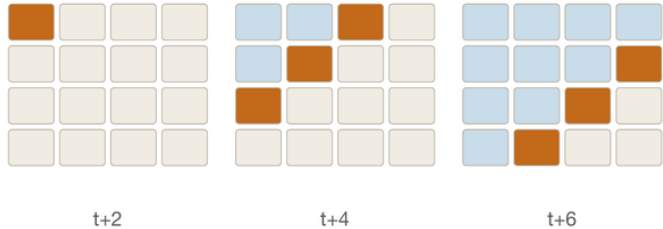
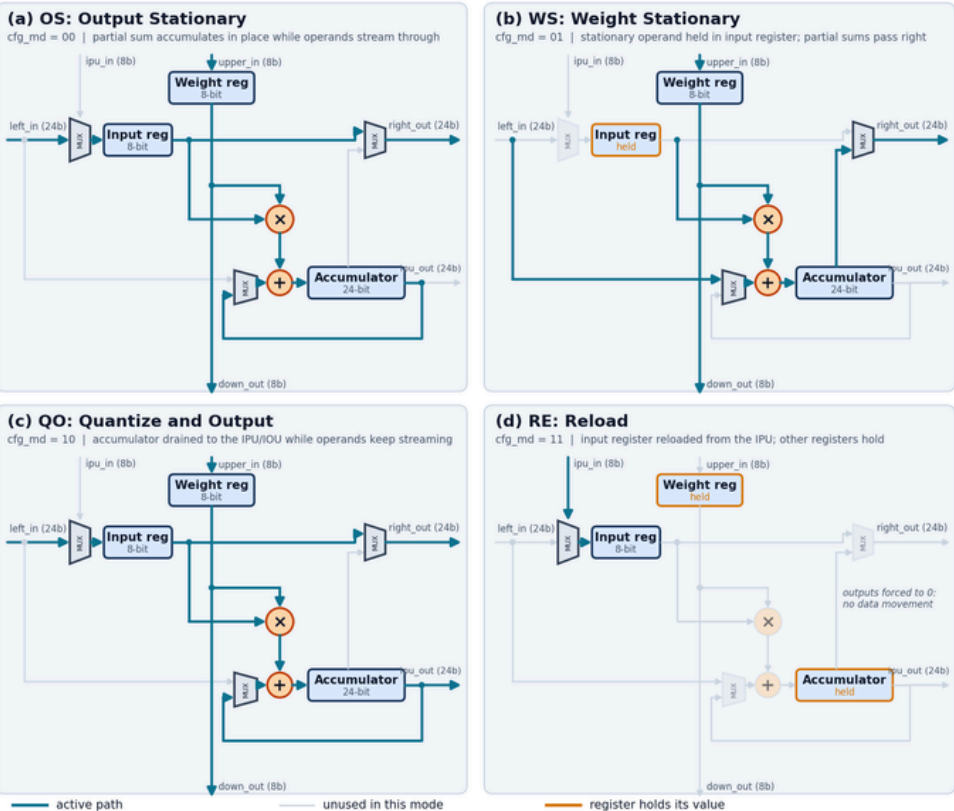


Systolic Array
Block Diagram

PEs on the same anti-diagonal switch mode together: PE(r, c) switches at $t = r + c + 2$
The mode wave is wired separately from the operand datapath, so its diagonal timing stays exact when operands stall.

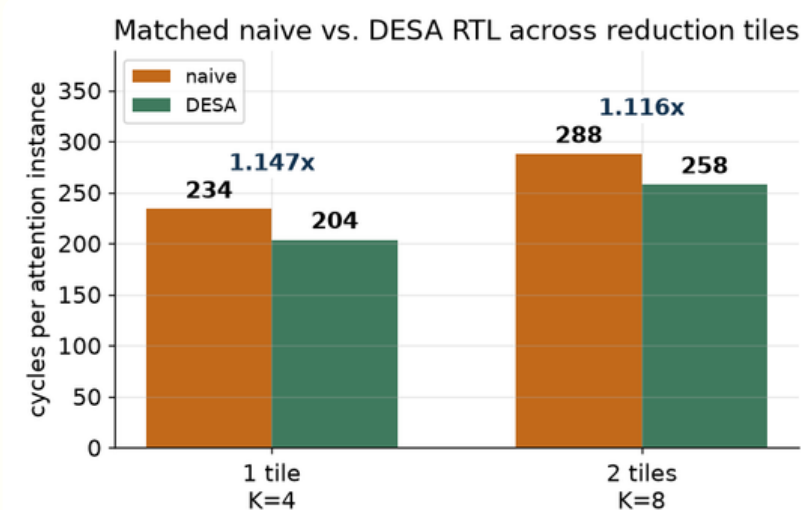
Configurable Processing Element (CPE): Four Runtime Modes

One multiplier, one accumulator, three data ports, and a 2-bit mode input (cfg_md) that selects the datapath

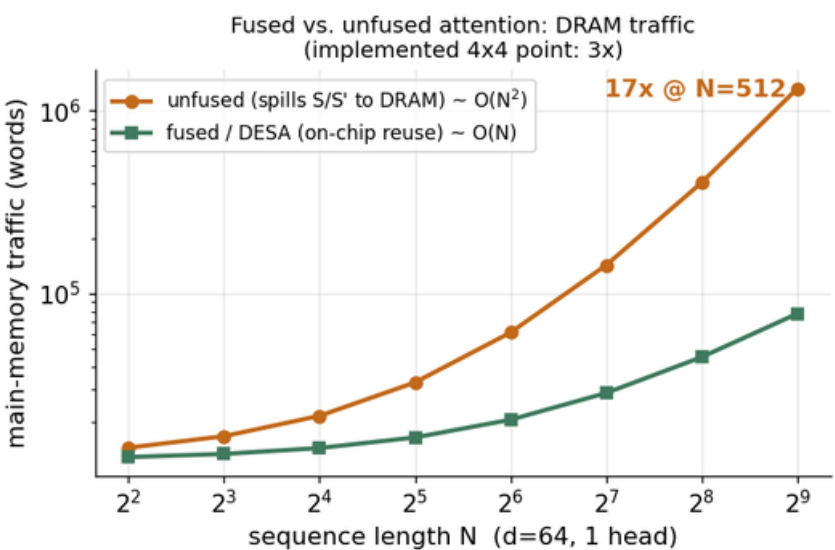


2D Mode Wave
Propagation Pattern

RESULTS



Measured Cycle Savings



Projected Full-Scale DRAM Traffic Savings

Resource Utilization

FPGA Implementation Results

Xilinx Spartan-7 xc7s25csga324-1 | Vivado 2025.1 | post-route, clock-only constraint

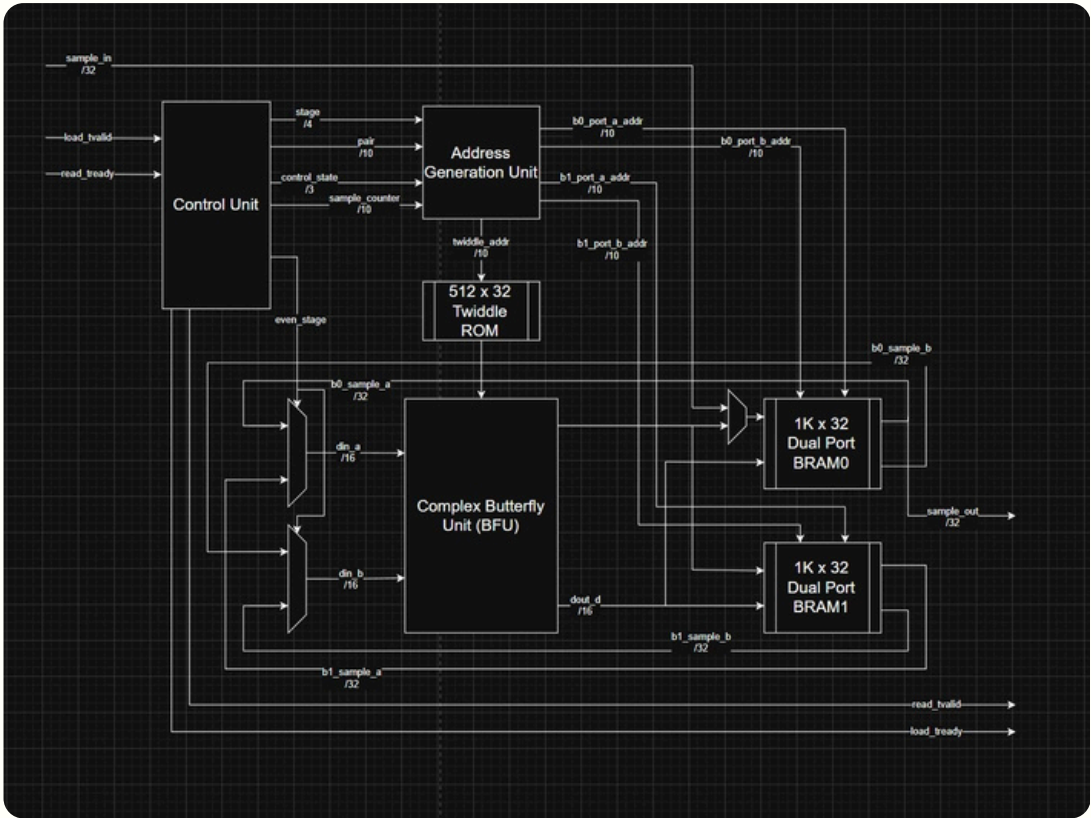
Resource Utilization				Timing (post-route)	
Resource	Used	Available	Utilization	Target clock	17.937 ns / 55.75 MHz
Slice LUTs	8,874	14,600	60.78%	Worst setup slack (WNS)	+0.019 ns
Slices	2,525	3,650	69.18%	Worst hold slack (WHS)	+0.159 ns
Slice Registers	2,247	29,200	7.70%	Worst pulse-width slack	+7.718 ns
F7 Muxes	161	7,300	2.21%	Failing endpoints	0 of 6,322
DSP48E1	10	80	12.50%	Critical path delay	17.863 ns
Block RAM Tiles	0	45	0.00%	logic / routing	31.8% / 68.2%
Distributed RAM only (428 LUTs as memory): the design uses no Block RAM.				logic levels	26 (10 CARRY4)
				Setup analyzed at the slow process corner.	

Critical path: mode-wave shift register → IPU running tile-max register
Internal register-to-register result; I/O delays were not constrained, so this is a core frequency, not a board-level limit.

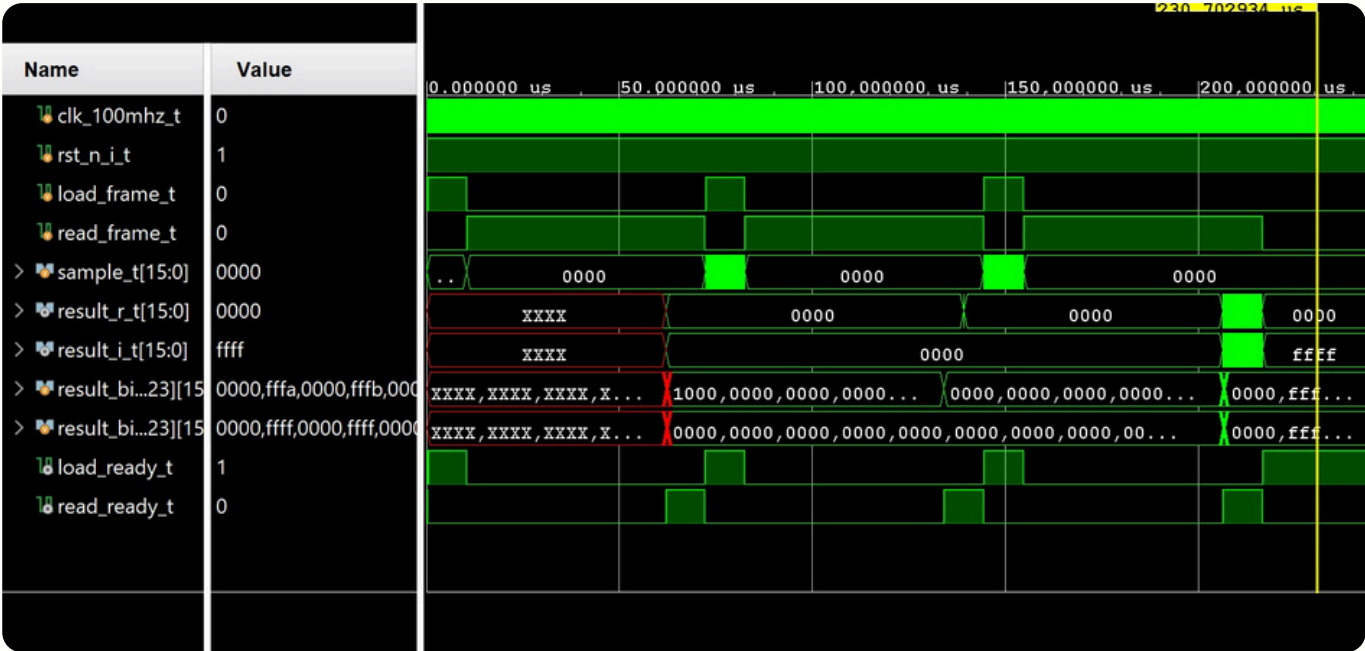
– Please see my website nickrathfelder.com for the full paper

FFT CORE

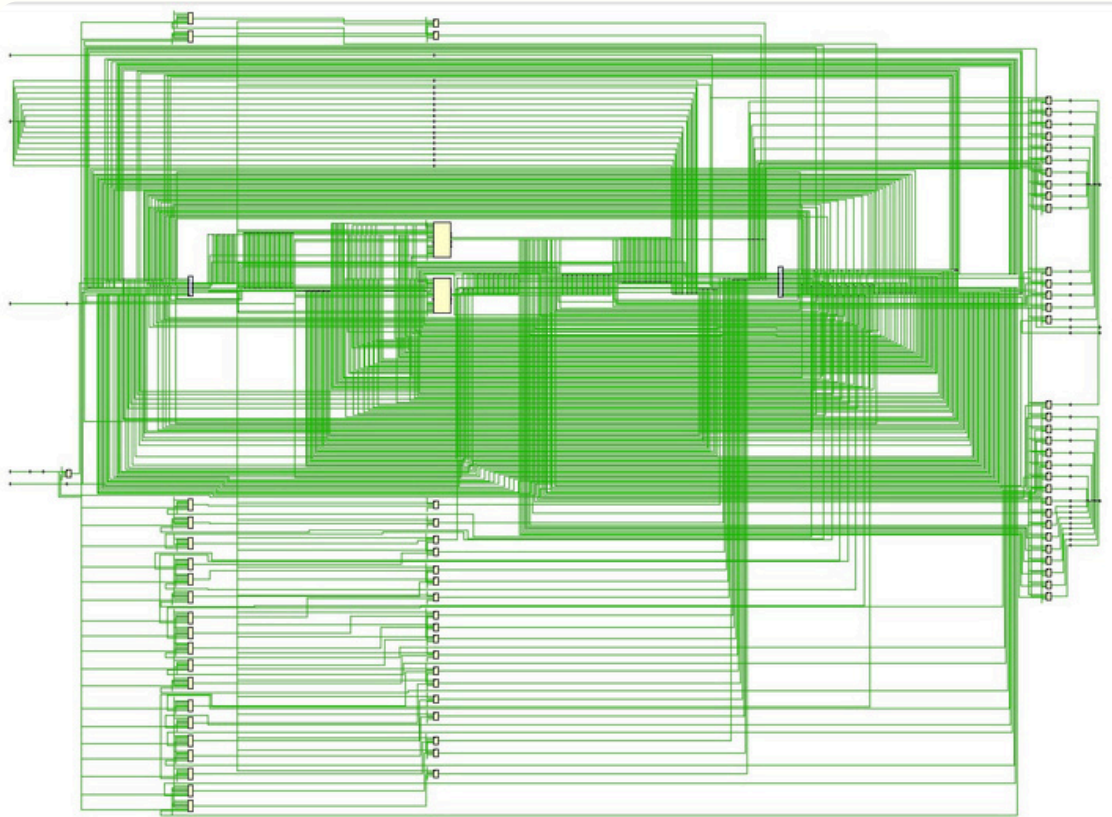
Top Level Block Diagram



Simulation Waveform

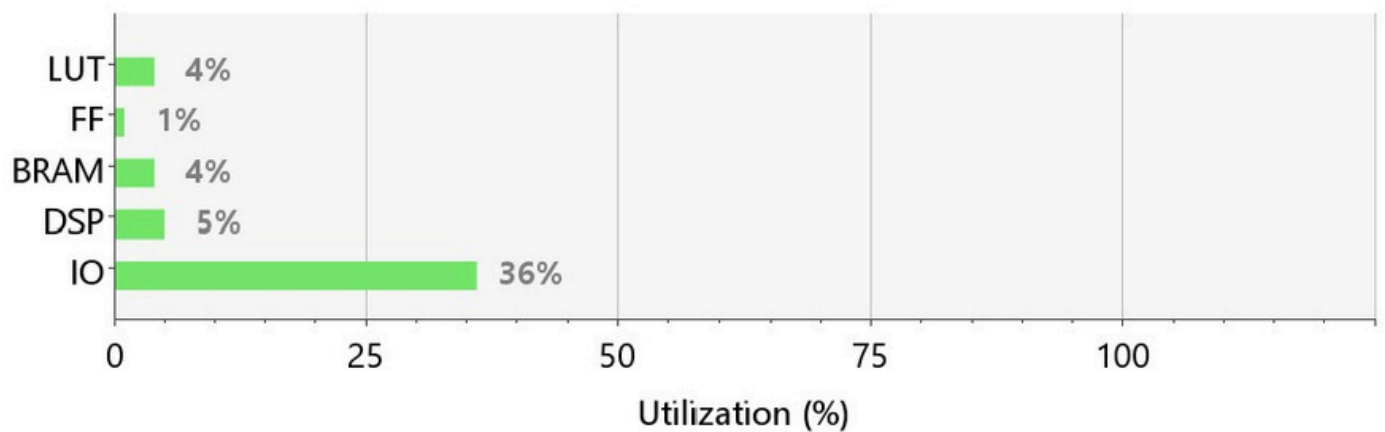


SYNTHESIS

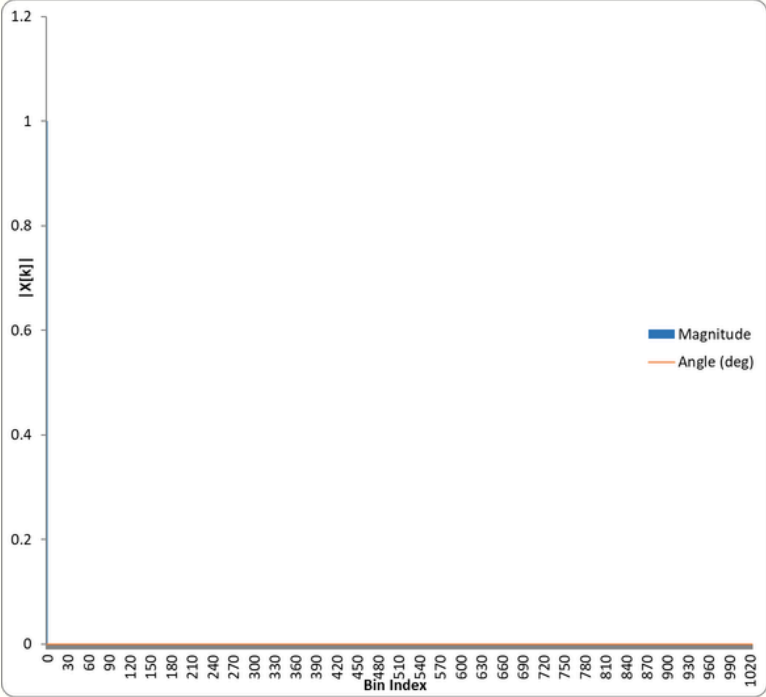


Synthesized
Design

Resource Utilization

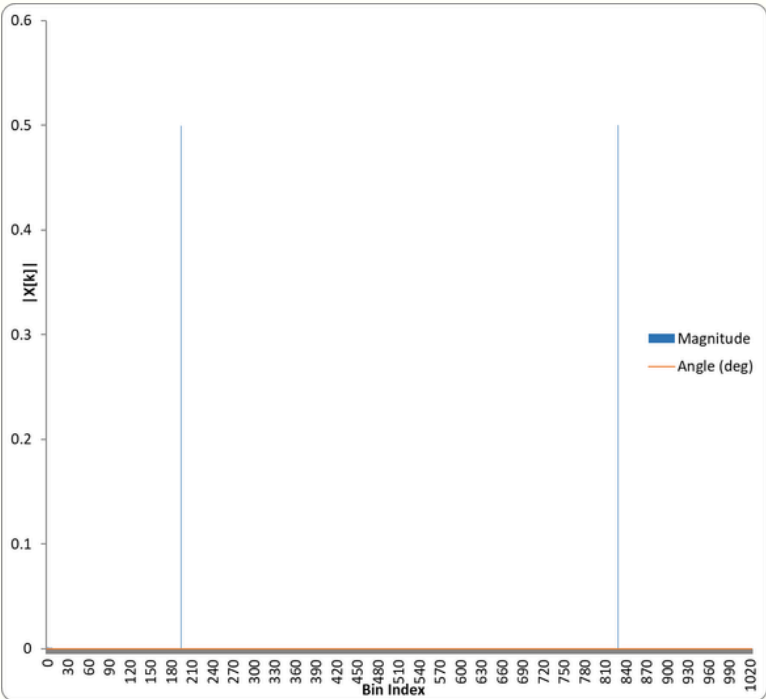
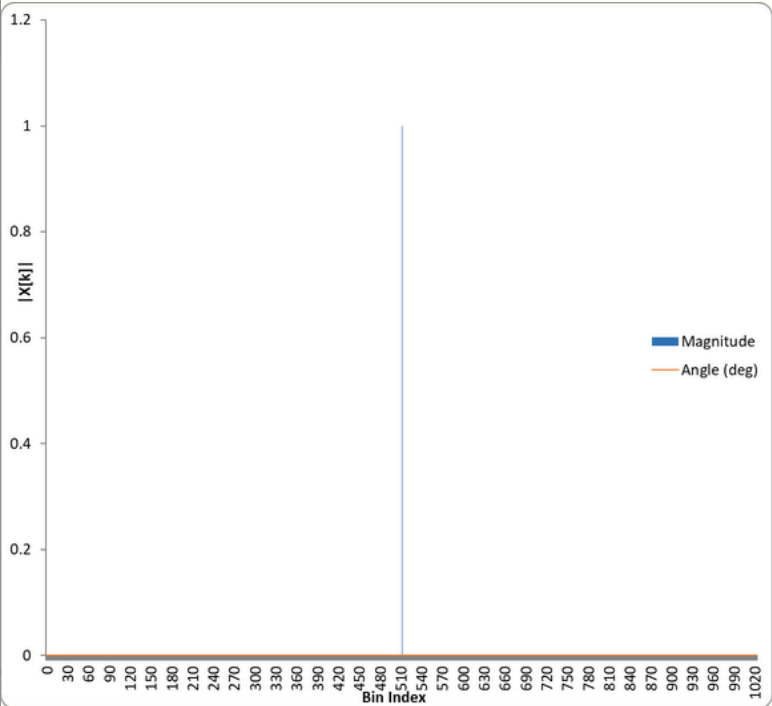


SIMULATION



Constant DC

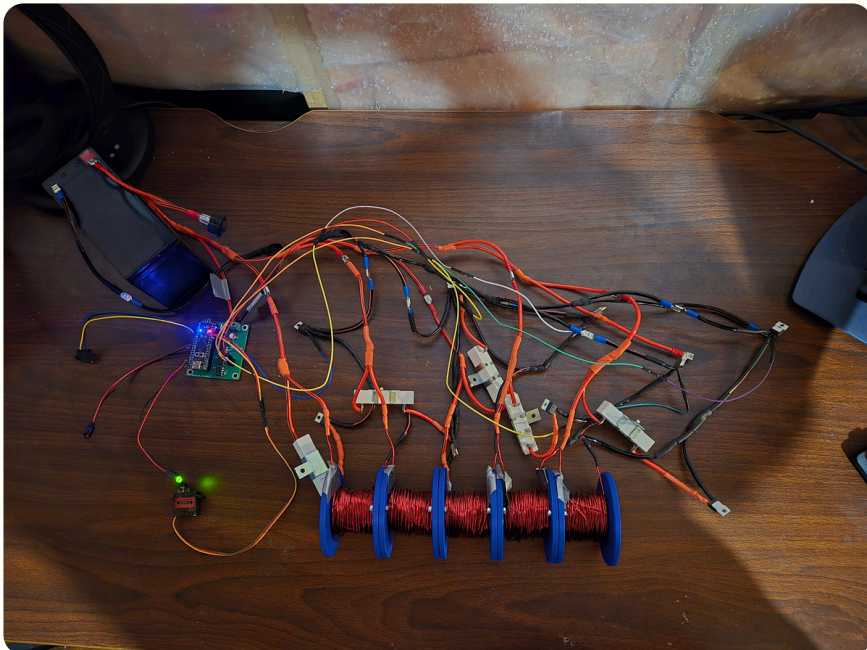
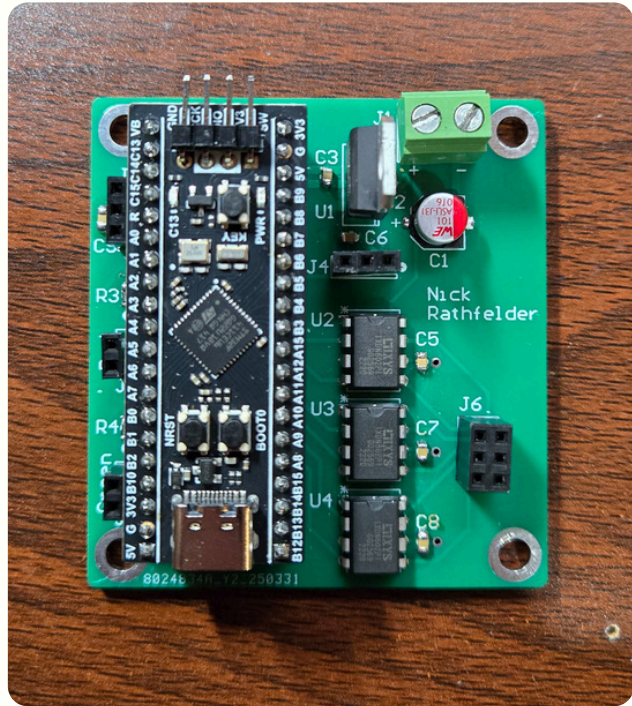
Nyquist
Sinusoid



Custom
Sinusoid
(Bin 195)

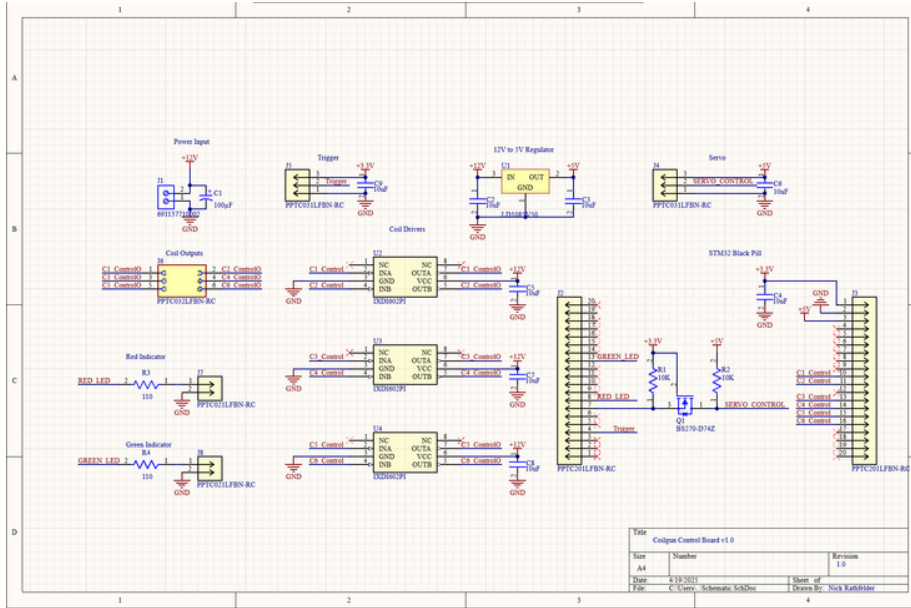
ELECTROMAGNETIC LAUNCHER

STM32
Interface PCB



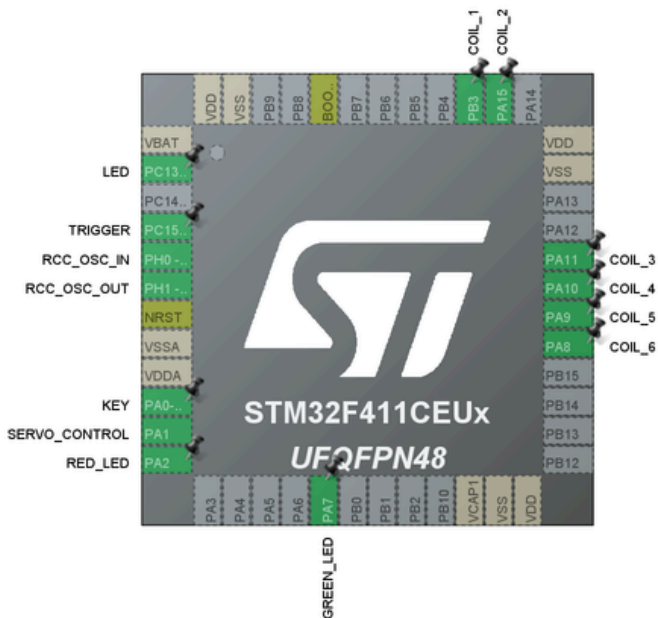
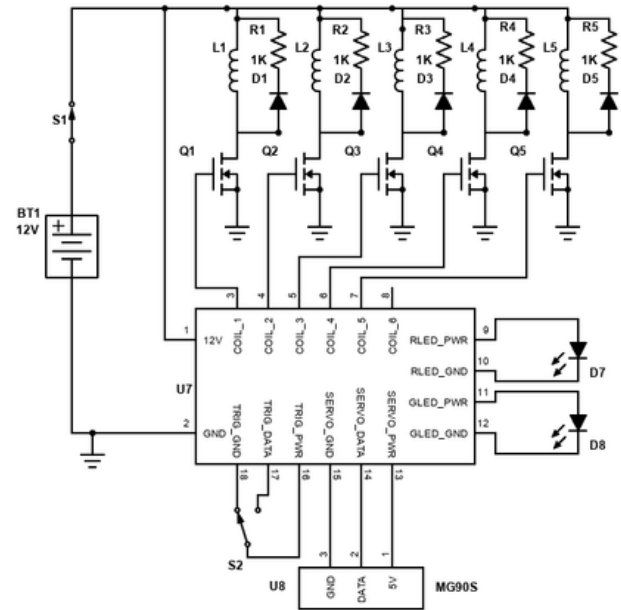
Final Prototype

DESIGN



Control PCB Schematic

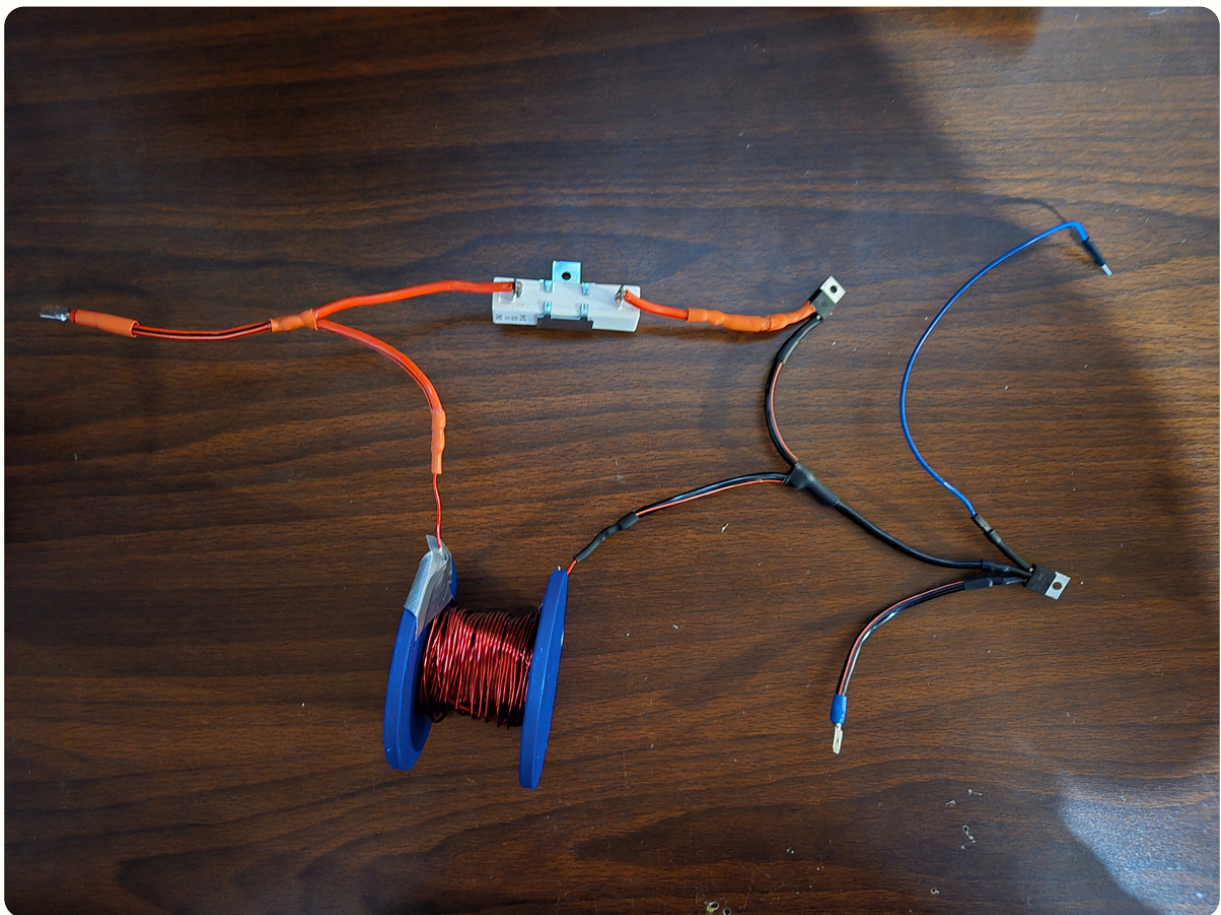
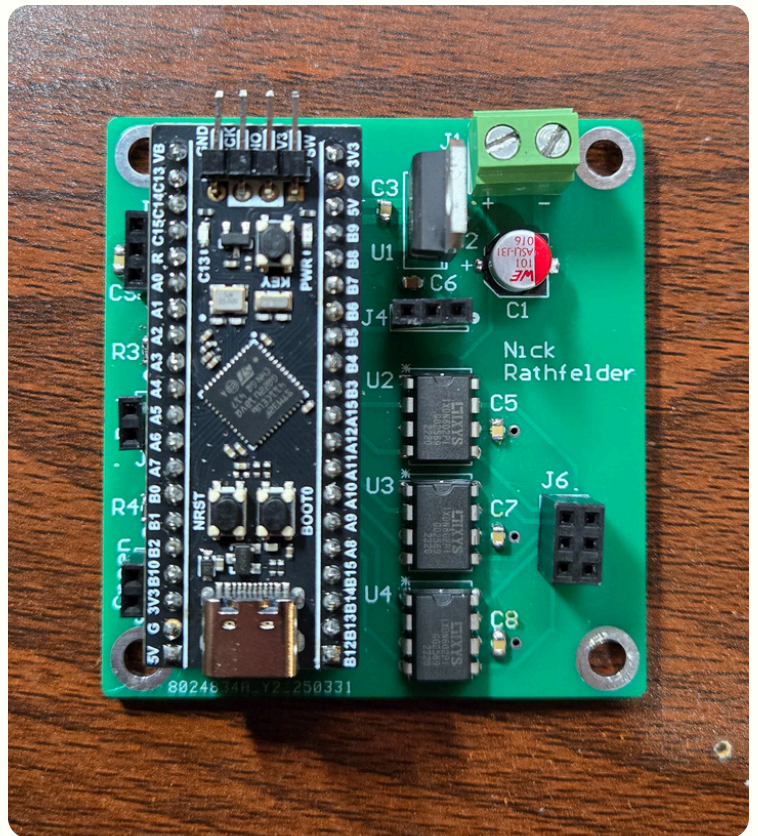
Wire Harness Schematic



MCU Pin Configuration

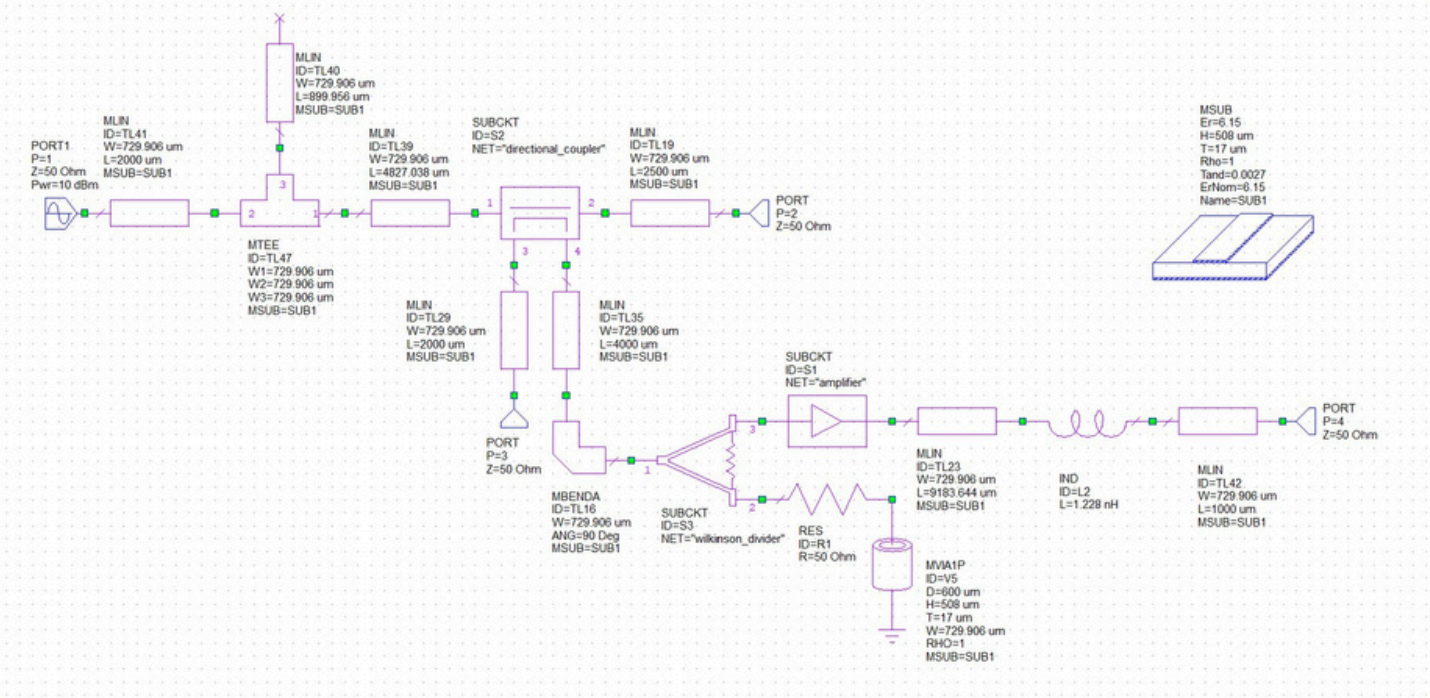
PROTOTYPE

Assembled
Control PCB



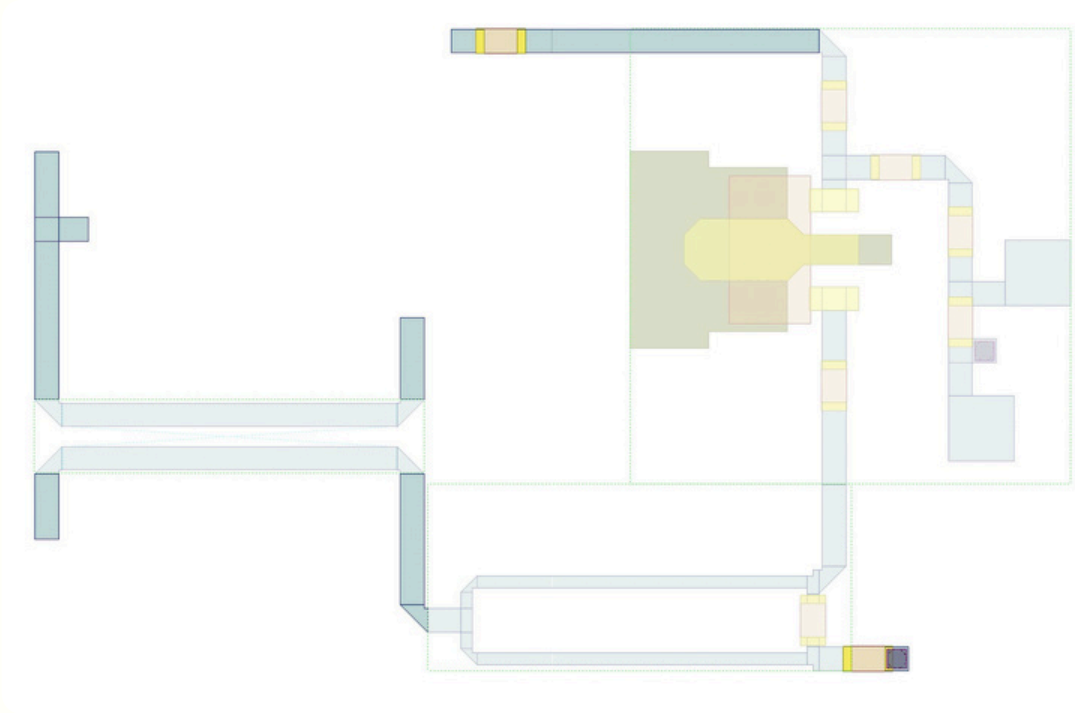
Single Coil Stage

RF REFLECTOMETER

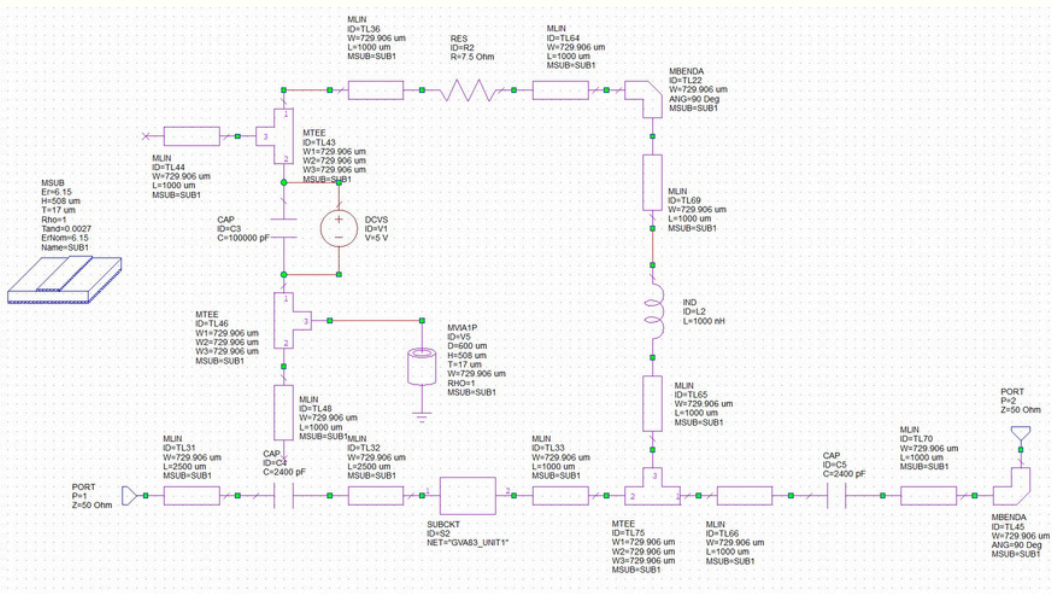
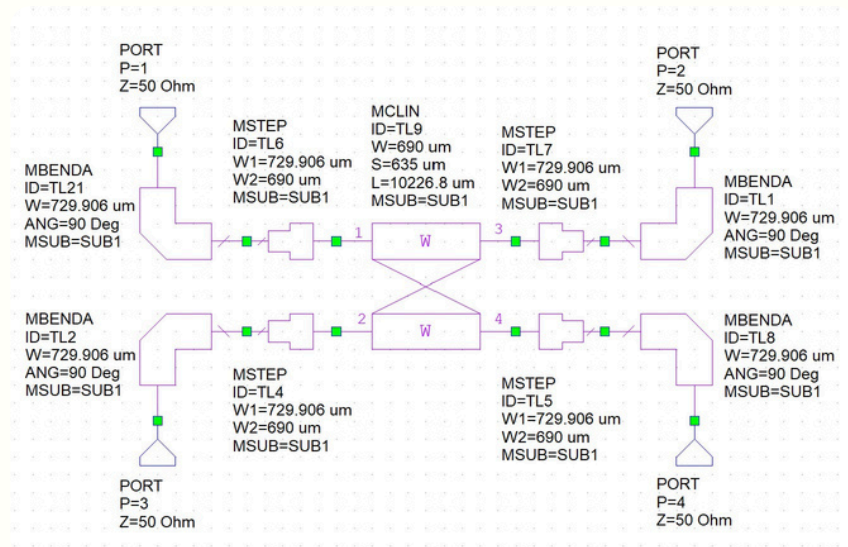


Top Level Schematic

Layout



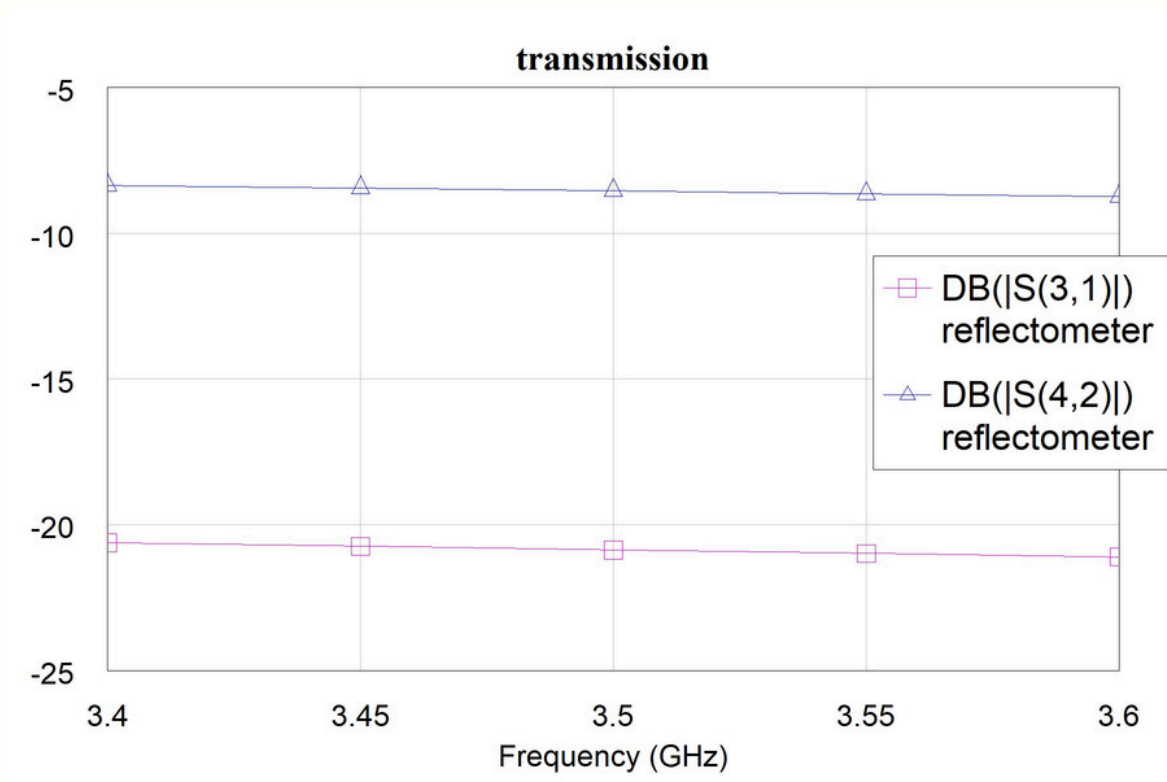
Directional Coupler



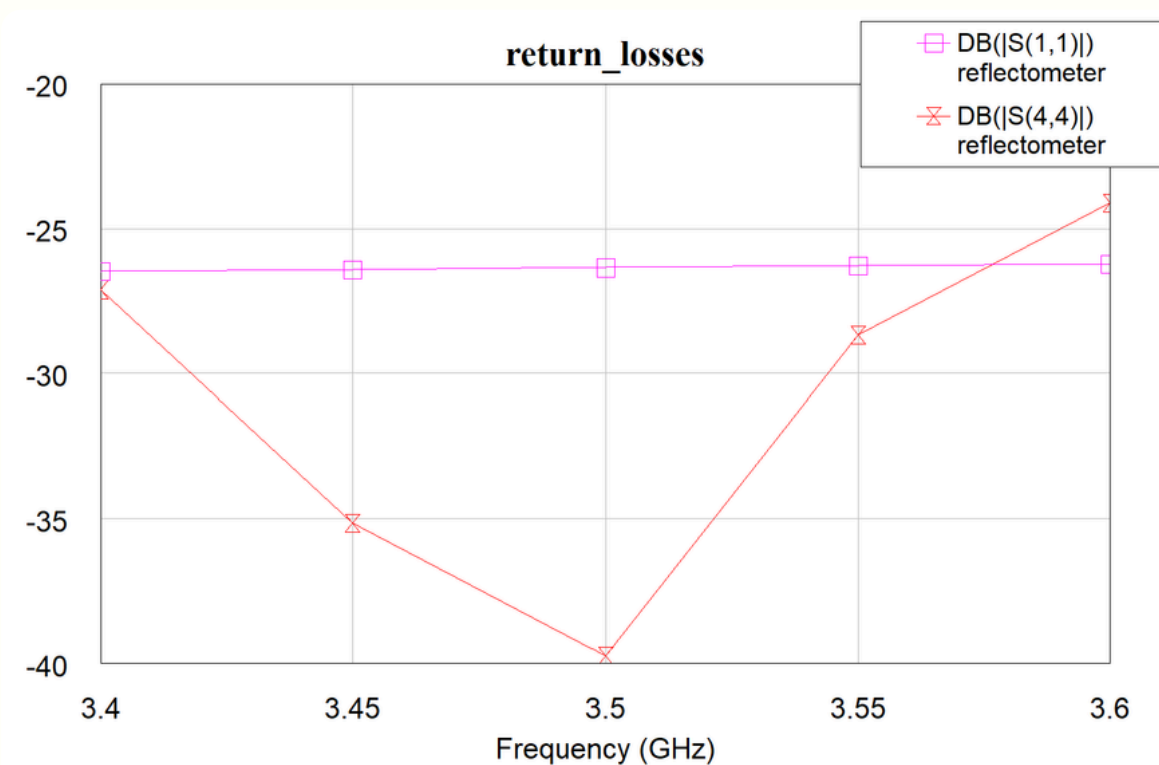
Amplifier

SIMULATION

Forward/Reflected Output Gain

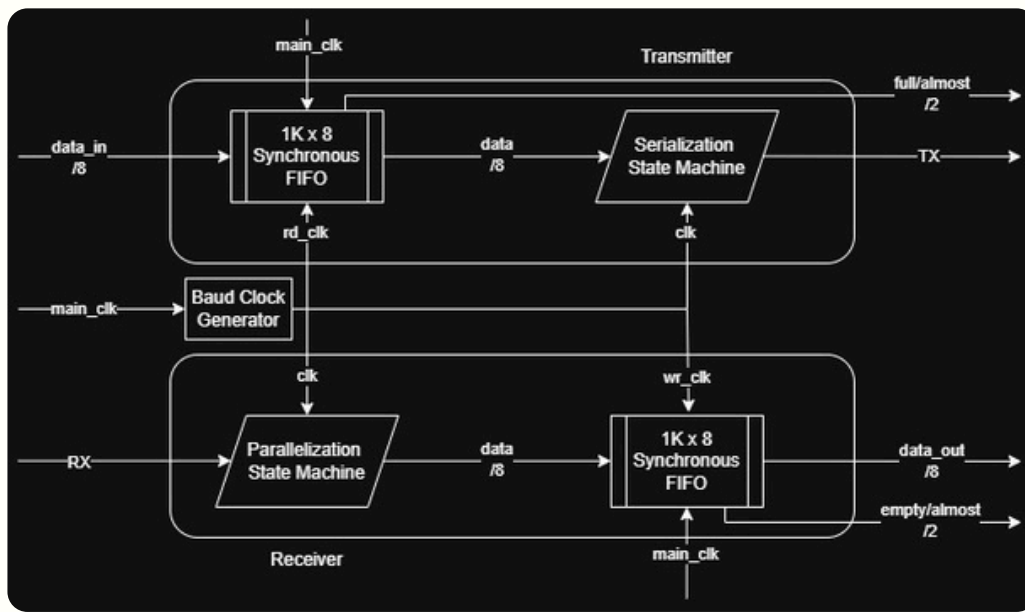


Input/Output Return Losses



SIDE PROJECTS

UART CORE + DEBUG PORT



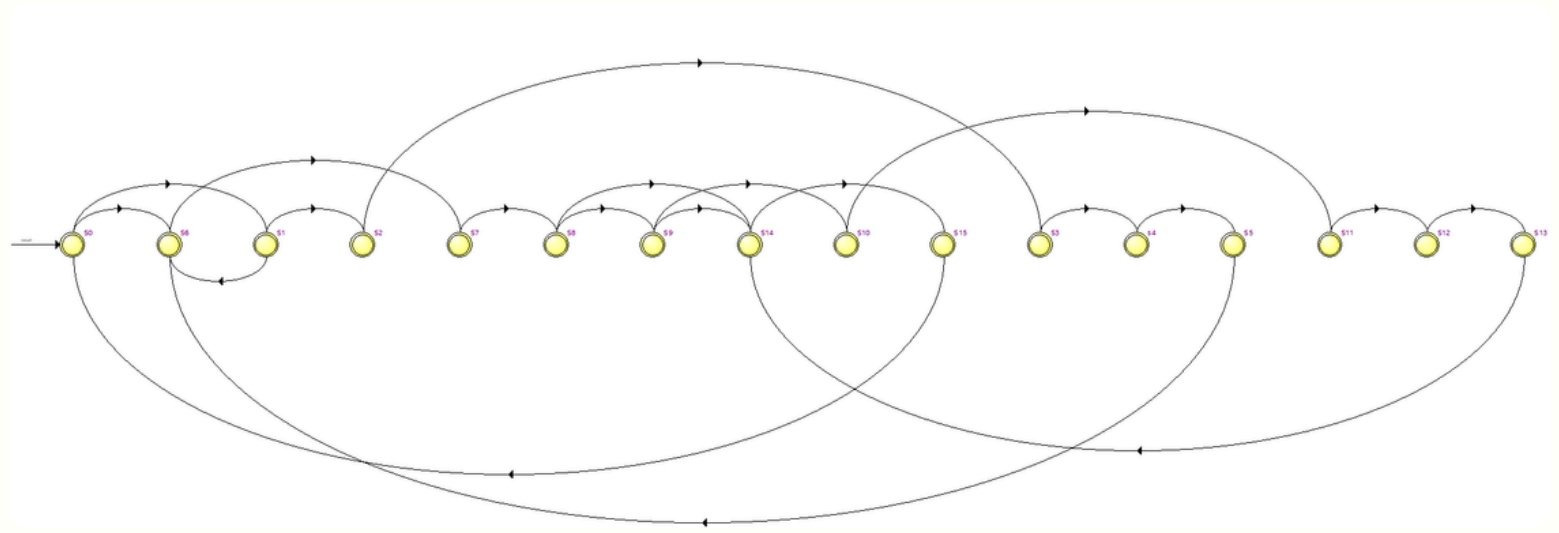
Block Diagram
(Core only)

Terminal
Output

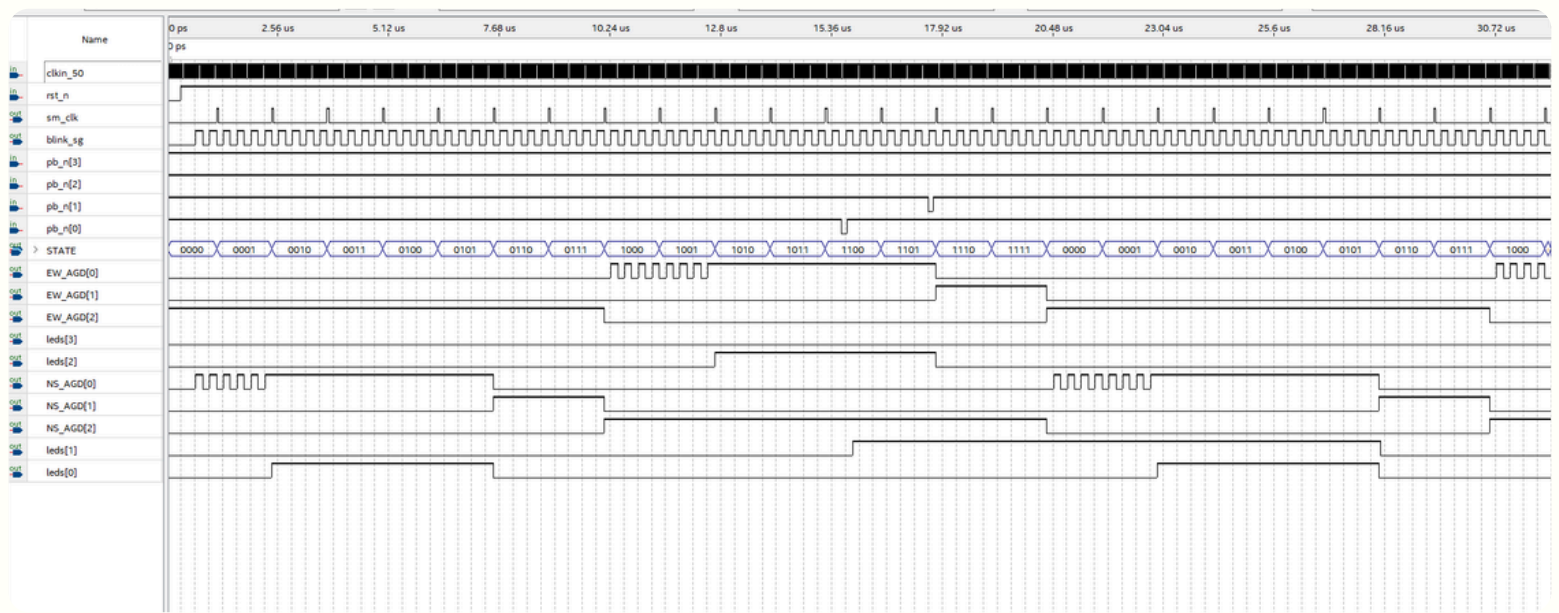
```
COM5 - Tera Term VT
File Edit Setup Control Window Help
MESSAGE_0_SENT
MESSAGE_1_SENT
MESSAGE_2_SENT
MESSAGE_3_SENT
MESSAGE_4_SENT
MESSAGE_5_SENT
MESSAGE_6_SENT
MESSAGE_7_SENT
MESSAGE_8_SENT
MESSAGE_9_SENT
MESSAGE_10_SENT
MESSAGE_11_SENT
MESSAGE_12_SENT
MESSAGE_13_SENT
MESSAGE_14_SENT
MESSAGE_15_SENT
```

FPGA TRAFFIC LIGHT CONTROLLER

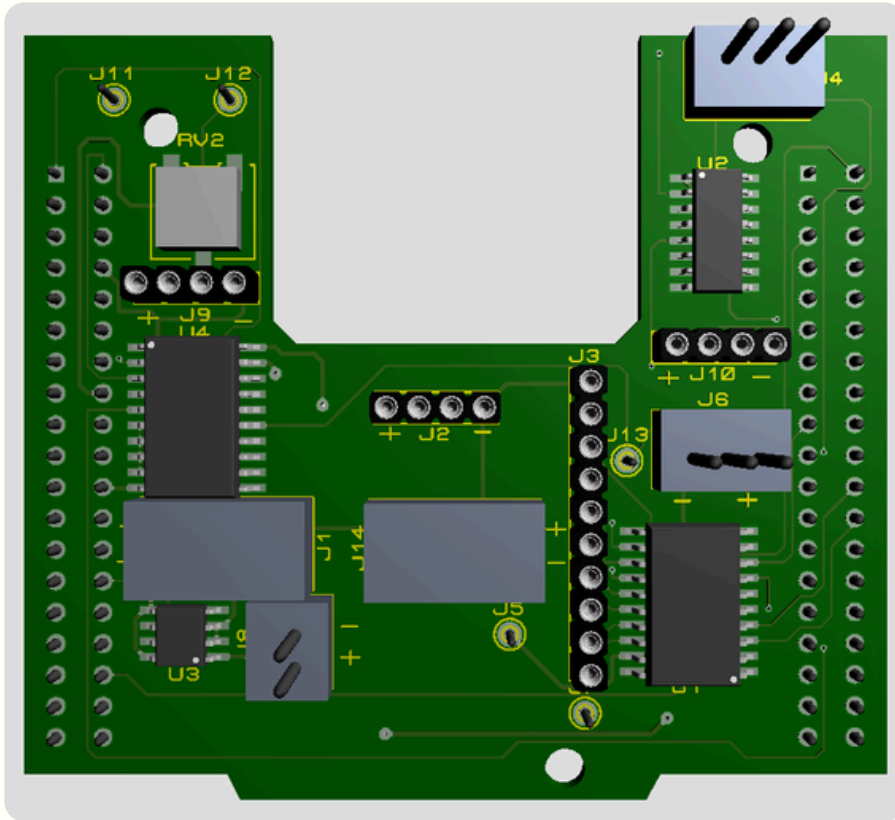
Controller State Machine



Testbench Waveform

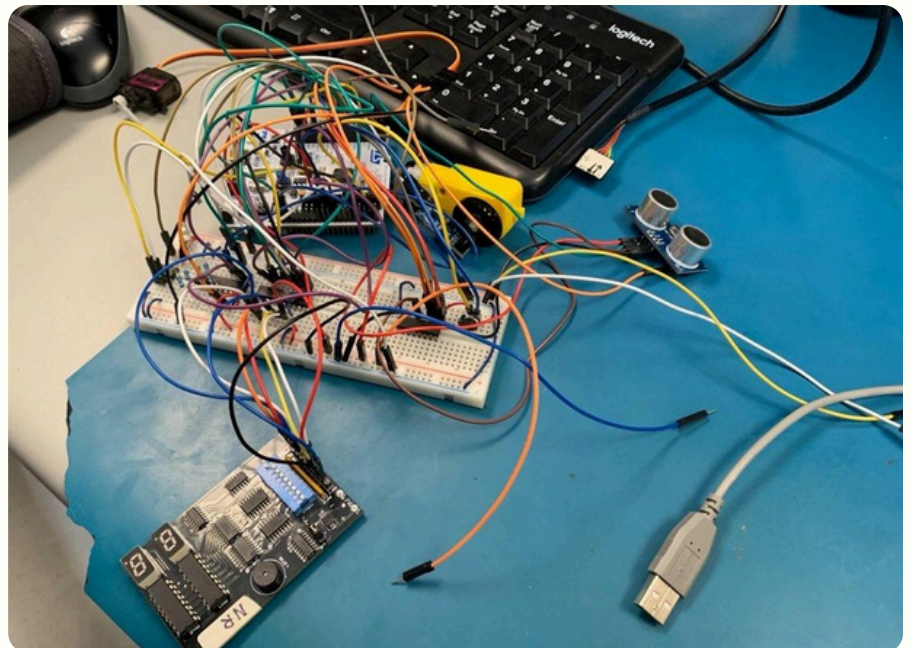


WATER RESERVOIR CONTROL SYSTEM



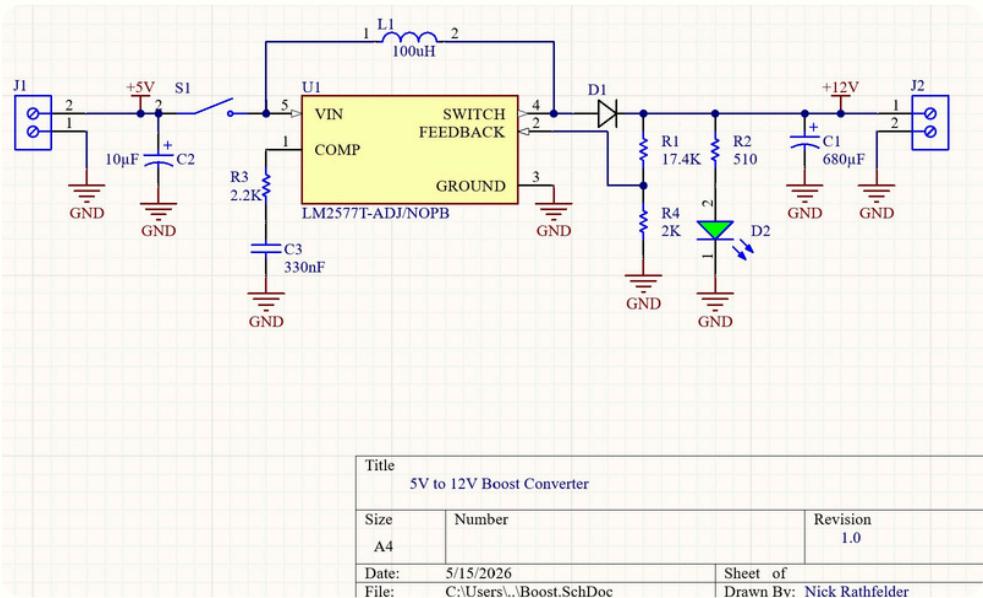
Interface PCB

Functional
Prototype

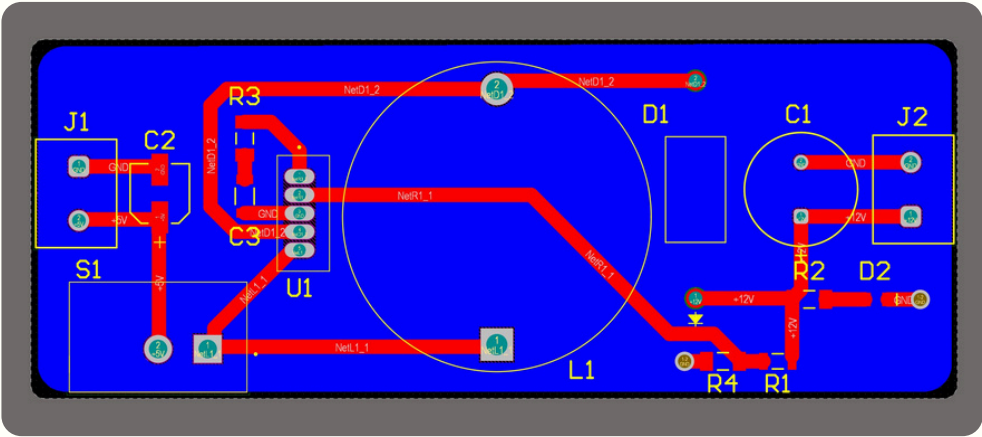


5V-12V BOOST CONVERTER PCB

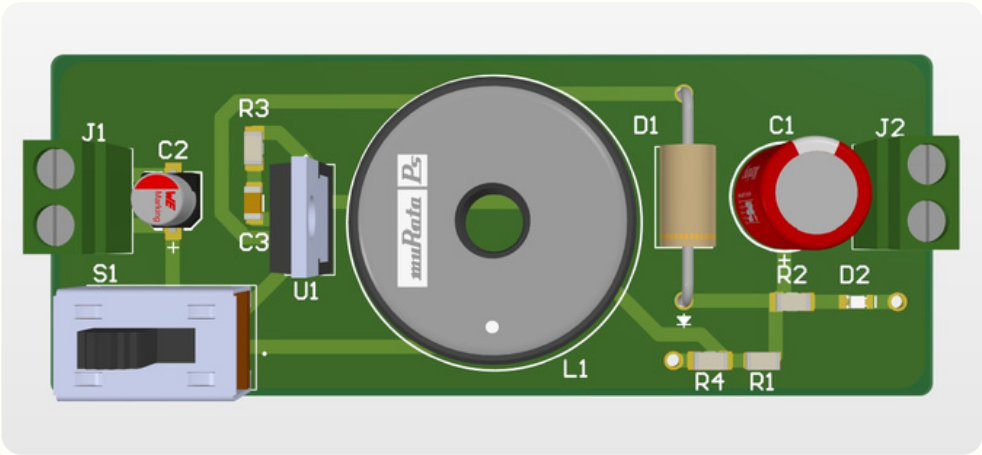
Schematic



Layout

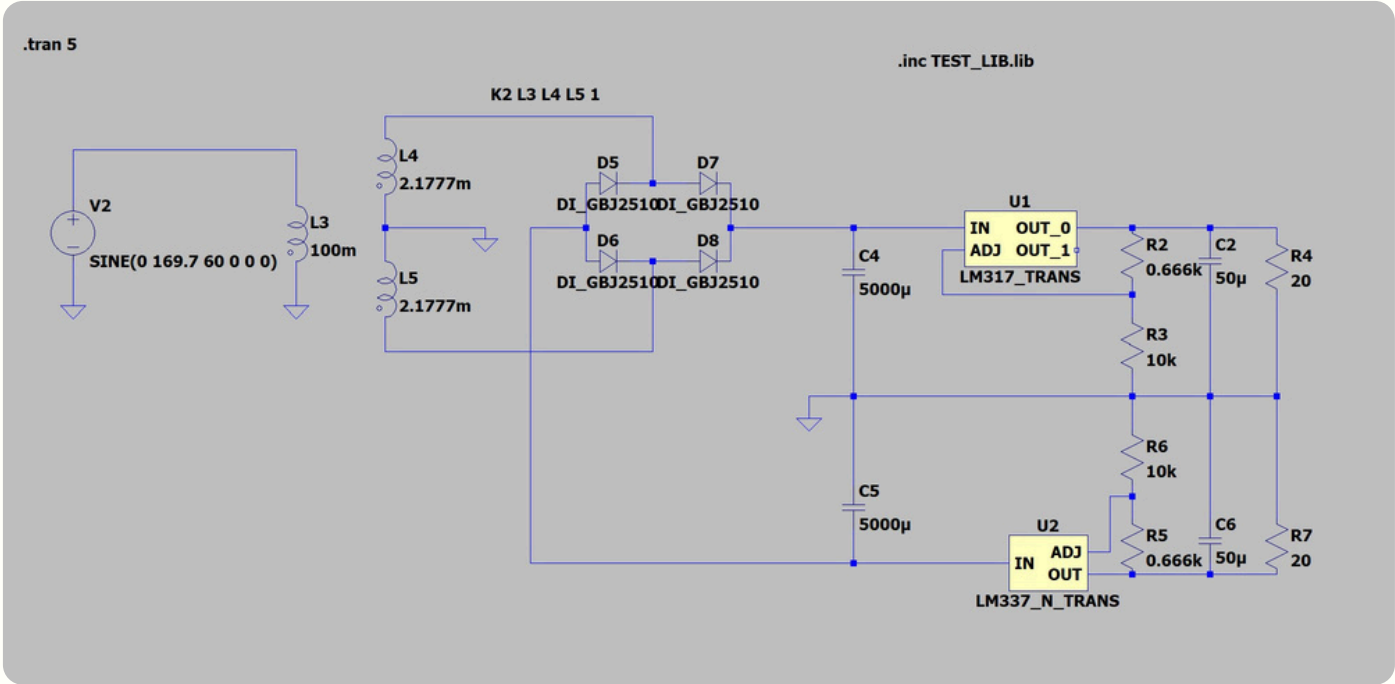


Model



SIMULATED DUAL OUTPUT AC-DC PSU

Schematic



Simulation

