

Nicholas Rathfelder

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Professional Summary

Fourth-year Electrical Engineering student with five co-op terms spanning RTL and FPGA design, memory-interface firmware, and transistor-level circuit design. Seeking digital or analog IC design roles.

Education

University of Waterloo, Term 4B

BASc in Electrical Engineering - 3.83/4 GPA

Relevant Coursework: Integrated Digital Electronics (CMOS), Electronic Circuits, AI/ML Hardware

Exchange Term (Winter 2026): Universidad Carlos III de Madrid (UC3M), Madrid, Spain

Waterloo

Sep. 2022 - Jun. 2027 (expected)

Technical Skills

Languages	SystemVerilog, Verilog, VHDL, C/Embedded C, C++, Python, TCL, Perl, MATLAB, ARM Assembly
EDA & Tools	Cadence Virtuoso, VCS, Vivado, Quartus Prime, Verilator, cocotb, LTSpice, Altium Designer, Cadence AWR
Hardware & Lab	Oscilloscope, Logic Analyzer, Vector Network Analyzer, LCR Meter, Waveform Generator, Soldering, Reflow Oven

Work Experience

Altera Corporation

IP Design Intern

Toronto, ON

Sep. 2026 - Dec. 2026

- Implemented DDR memory calibration firmware, running and analyzing VCS RTL simulations to validate it against the design
- Retargeted LPDDR5 calibration firmware and regression tests to LPDDR4 per JEDEC timing requirements, debugging 6 failing tests

Curtiss-Wright Defense Solutions

FPGA Engineering Intern

Kanata, ON

Sep. 2025 - Dec. 2025

- Designed RTL for a UART debug interface exposing internal hardware states during restricted-access environmental testing
- Integrated third-party IP and supported simulation and testing of FPGA designs for mission-critical aerospace and defense systems

Musashi AI

Controls and Electrical Engineering Intern

Waterloo, ON

Jan. 2025 - Apr. 2025

- Updated electrical drawings and developed PLC/robot programs for AI automotive inspection machines
- Upgraded the Automate 2025 tradeshow inspection cell to add onboard chatter inspection of automotive camshafts

Martinrea International

Electrical Engineering Intern

Tillsonburg, ON

Sep. 2023 - Dec. 2023

- Implemented an AI weld inspection system designed to cut cycle time by over 25%
- Integrated GPIO-triggered serial messaging into the in-house weld inspection system, improving response time

Stelco - Lake Erie Works

Process Engineering Intern

Nanticoke, ON

Jan. 2023 - Apr. 2023

- Built Power BI reports giving the Hot Strip Mill operating team visibility into daily operations
- Began developing a MATLAB and PLC image-analysis tool to monitor slag buildup on basic oxygen furnace walls

Projects

16-bit CMOS Carry-Lookahead Adder

Transistor-level 16-bit adder using two-level carry lookahead, designed for 1 ns addition time across all corners

Cadence Virtuoso

Spring 2026

- Implemented in 45 nm static CMOS from four 4-bit lookahead blocks and a second-level carry generator, verified across corners
- Cut nominal worst-case delay from 1008 ps to 456 ps versus a ripple-carry baseline, with 676.5 ps at the slowest corner (SS, 85 °C)

Runtime-Configurable Systolic Array for Transformer Acceleration

Reduced-scale RTL accelerator for transformer attention, with runtime-switchable dataflow and on-chip operand reuse

SystemVerilog, cocotb, Verilator

Spring 2026

- Designed RTL for a 4×4 INT8 systolic array with four runtime dataflow modes and a diagonal mode-wave register for staggered transitions
- Enabled on-chip query reuse, saving 30 cycles per attention operation (1.147×), verified bit-exact with cocotb

Awards and Honours

Aug. 2026

Honour: Term Distinction in 2A, 2B, 3A, 4A

Aug. 2022

Scholarship: WatPD Engineering Entrance Scholarship